REV	ZONE	ECO #	REVISION	APPD	DATE
A		C288	INITIAL RELEASE		
A		F115	CHANGED TEST PROGRAM LIMITS	BCS BWLO	4/14/83
A		F221	PAGE 2: ADDED WARNING SECTION	[illegible]	[illegible]
B		J061	Page 7: Added Windowing (paragr.3)	[illegible]	[illegible]

DRAWING NUMBER 343-0041-B

SH 1 OF 14

PRODUCTION RELEASE

[illegible] PROPERTY

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMALS .X ± ___ .XX ± ___ .XXX ± ___ ANGLES XX.X ± ___ FRACTIONS ± ___ DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.	DRAWN BY A. B DATE 1/83 CHECKED BY [illegible] DATE 1/83 APPROVED BY [illegible] DATE 1/83 RELEASED BY [illegible] DATE [illegible]	apple computer inc.	
		TITLE IC, INTEGRATED, WOZ MACHINE (IWM)	
MATERIAL: ———		SIZE A	DRAWING NUMBER 343-0041-B
NEXT ASSY.	FINISH: ———	SCALE: ———	SHEET 1 OF 14

Integrated WOZ Machine (IWM)

Device Specification

Features

* Backwards-compatible with 16 sector Disk][controller
* Use of 7M (or 8 mHz) to minimize sampling error rate
* Fast mode using 2 uS bit cells
* Asynchronous mode with pollable handshake registers

WARNING

The IWM will not work reliably in synchronous mode with the 6502 using Apple II disk software. It will work with the CMOS version done by Western Design Center (NCR supplies this part as NCR65C02).

During the load accumulator instruction, if the D7 output of the IWM changes to 1 just before the end of the microprocessor read window, the NEGATIVE flag may be set but A[7] remain 0. This results in recognition of a "valid" byte. The accumulator will contain the byte except A[7] will be incorrect The difference between the 6502 and the 65C02 is that the latter uses regenerative feedback to force the latched input data to valid logic levels after the read window ends. This guarantees the NEGATIVE flag and A[7] will be equal after the load accumulator instruction.

The 6502 may be used if A[7] is not used in the de-nibblizing process. A simple fix to the current routines is to force A[7] to a 1 by ORA #$80 after reading the nibble.

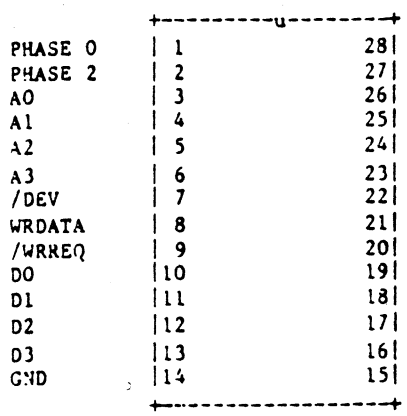
General Description

The IWM is an integration of the Disk II floppy disc interface. When the IWM is reset, it becomes a controller compatible with the current Disk II interface in its operation with currently supported Apple II nd /// software. In addition, the IWM has extensions including a status register, mode register, and multiple modes of operation. The IWM provides an asynchronous mode, a fast mode with a data rate twice that of Disk II, and an optional 1 second one-shot timer to hold the enable outputs low.

The IWM is a peripheral device that connects to a host data bus. The device generates and receives serial GCR encoded data. A programmable digital one shot is used for serial data recovery. The IWM generates buffered drive enables and phase line control outputs.

Packaging and Pin Assignment

The IWM is packaged in a standard 28 pin, 600 mil plastic DIP.



An underrun occurs when data has not been written to the buffer register between the time the write-handshake bit indicates an empty buffer and the time the buffer is transferred to the write shift-register. If an underrun occurs in asynchronous mode /WRREQ will be disabled (set to a TTL high state) and the /underrun flag will be set to zero. This occurrance can be detected by reading the write-handshake register before clearing state bit L7. Clearing state bit L7 will reset the /underrun flag.

When L6 and L7 are both zero the IWM is in the read state. When reading serial data, a falling transition within a bit cell window is considered to be a one, and no falling transition within a bit cell window is considered to be a zero. The receive data input on RDDATA is synchronized internally with the CLK clock. The synchronized falling transition is then discriminated to the nearest bit cell window using the 7/8 mHz FCLK clock signal in fast mode and the FCLK signal divided by two in slow mode. A digital one-shot data recovery scheme is used. Every falling transition establishes the bit cell windows, used by the data separator in the IWM to recover the following bits, until another falling transition is received.

The B revision adds windowing such that after each falling transition of RDDATA there is a window during which subsequent falling transitions are ignored. In 8M FAST mode this window is 6 FCLK periods, while in 7M FAST mode it is 5 FCLK periods. For SLOW mode the windowing is twice as long. Since RRDATA is synchronized to FCLK in FAST mode there is one FCLK uncertainty as to whether a transition is within the window or not. In SLOW mode this uncertainty is 2 FCLK periods. Thus for 8M FAST mode a falling transition spaced less than 750ns will be ignored, those between 750ns and 875ns will sometimes be ignored, and those greater than 875ns will be detected. For 7M SLOW mode a falling transition spaced less than 1.4us will be ignored, those between 1.4us and 1.68us will sometimes be ignored, and those greater than 1.68us will be detected.

In the read state the data is shifted into the LSB of the shift register, and the shift register shifts data from LSB to MSB. A full data nibble is considered to be shifted in when a one is shifted into the MSB. When a full data nibble is shifted into the internal shift register, the data will be latched by the read data register and the shift register will be cleared to all zeros so that it will then be ready to shift in the next data word.

In the synchronous mode the shift register is readable in any intermediate state with this exception: when a one is shifted into the MSB, the shift register will appear, to the data bus, to be stalled for a period of two bit times plus four CLK periods. This is to allow the host processor time to poll the MSB to determine when data is valid. In asynchronous mode the data register will latch the shift register when a one is shifted into the MSB and will be cleared 14 FCLK periods (about 2 uS) after a valid data read takes place (a valid data read being defined as both /DEV being low and D7 (the msb) outputting a one from the data register for at least one FCLK period).

Technical Description

The primary purpose of the IWM is to allow a microprocessor to read and write serial GCR (group code) encoded data. The IWM may be controlled by setting state bits and reading or writing registers. Setting a state bit and accessing a register is done simultaneously. The registers are the mode register, the status register, the write-handshake register, the read data register, and the write data register. The modes selected by the mode register include synchronous or asynchronous mode and slow or fast mode.

The data format is an 8 bit nibble with the MSB set. The MSB of the 8 bit data nibble is shifted in or written out first. A bit is transferred every bit cell time. The bit cell time defaults to 4 uS (set to 2 uS in fast mode). Therefore the data rate is one nibble every 32 uS (16 uS in fast mode). When writing data out, a one is written as a transition on the WRDATA output at a bit cell boundary time and a zero is written as no transition.

The IWM is put into the write state by a transition from the write protect sense state to the write load state. In the synchronous mode, the time of that transition and every 8 Q3 periods (4 uS) thereafter, until L7 is cleared, marks the beginning of a write window. The duration of the write window is 4 periods of the Q3 input signal (2 uS). The data written at the last write access occurring within this write window will load the shift register with the data to be shifted out. If the next write access has not occured 32 uS (64 Q3 periods) after a load, the write will be extended in multiples of 4 uS (8 Q3 periods) until another write access, and zeros will be shifted out.

In synchronous mode, Q3 clock input is used internally to generate the 32 and 40 uS timings, which would then be 64 and 80 of the Q3 clock input periods in duration, respectively, and the bit cell timings, 8 Q3 periods per bit cell time in slow mode.

In asynchronous mode the write shift register is buffered and, when the buffer is empty, the IWM sets the MSB of the write-handshake register to a one to indicate that the next data nibble can be written to the buffer. The buffer register may be written at any time during the write state. Only the data last written into the buffer register, before the contents of the buffer register is transfered to the write shift register, is used.

In asynchronous mode CLK is used to generate the bit cell timings. In fast mode the CLK clock is equivalent to the clock input on FCLK. In slow mode CLK is equivalent to the clock input on FCLK divided by two. Therefore, in 7M and slow mode the bit cell time will be 28 FCLK clock input periods in duration, in 8M and slow mode the cell time will be 32 periods, and in 8M and fast mode the cell time will be 16 periods. In asynchronous mode the write shift register is loaded every 8 bit cell times starting seven CLK periods after the write state begins.

Read data bit cell windows

mode		Nclks	period	data	notes
slow	7M	7-2Ø	FCLK/2	1	2.Ø-5.71+ uS
		21-34		Ø1	6.Ø-9.71+ uS
		35-48		ØØ1	1Ø.Ø-13.71+ uS
					window is 28 clks
slow	8M	8-23	FCLK/2	1	
		24-39		Ø1	
		4Ø-55		ØØ1	
fast	7M	7-2Ø	FCLK	1	window is 14 clks
		21-34		Ø1	
		35-48		ØØ1	
fast	8M	8-23	FCLK	1	1.Ø-2.875+ uS
		24-39		Ø1	3.Ø-4.75+ uS
		4Ø-55		ØØ1	5.Ø-6.875+ uS
					window is 16 clks

The table above shows how the data separator in the IWM discriminates between ones and zeros when reading. Nclks is the number of clock periods between falling transitions of the internally synchronous version of RDDATA. The clock period is either that of the FCLK input or that of the FCLK input divided by two in slow mode. Each falling transition resets the read data windows for subsequent data to be relative to that transition. The data patterns noted above are the bit patterns that are shifted in as a result of the transitions and the absence of transitions in their respective windows.

In port operation, which is asynchronous mode true and latch mode false with /DEV held low indefinitely, read data will appear and change as if the IWM were being continually read. In port operation the MSB can be used to continously clock data into external registers. The MSB will be cleared at least six FCLK periods before being set. Except in port operation, in asynchronous mode the latch mode bit should be set (for reliability in clearing the data register after a read).

Data written to the IWM is sampled by the zero to one transition of the logical OR of Q3 and /DEV . In asynchronous mode the Q3 input may be tied low.

Signal and Bus operation Description

1. Vcc — +5 volt supply
   GND — Ground reference and negative supply

2. Device Control Signals

A1-A3	These three inputs select one of the 8 bits in the state register to be updated.
AØ	The data input to the state bit selected by A1-A3. The state to which the addressed state bit is set by an operation will select the register to be accessed by that operation. Also the /READ input. A low on this input enables the IWM to send the register selected by the state onto the data bus.
DØ-D7	The bidirectional data bus .
/DEV	Active low device enable. The falling edge of /DEV latches information on AØ-A3. The rising edge of the logical function (Q3 OR /DEV) qualifies write register data.
FCLK	Clock input for the serial data logic; either 7 or 8 MHz.
Q3	2.Ø Mhz clock input used to qualify the timing of the serial data being written out in the synchronous mode.
/RESET	Active low system reset input. When asserted, this signal places all IWM outputs in their inactive state, and sets the state and the modes to their defaults.

3. Inputs (2)

RDDATA	The serial data input. The falling transition of each pulse is synchronized by the IWM.
SENSE	An input to the IWM that can be polled via the status register.

4. Outputs (8)

WRDATA	The serial data output. A transition occurs on this output for each one bit.
/ENBL1 , /ENBL2	Programmable buffered output lines. No more than one enable may be low at any time. If an enable is low than Motor-On is true. If the 1-second on board timer is enabled then the selected one will stay low for about 1 second after it is programmed high.
/WRREQ	This signal is a programmable buffered output line.
PHASEØ-3	These are programmable output lines. A true TTL logic "1" (2.4 volts) can be maintained even while driving two darlington inputs in parallel.

Register Description

State Register

This is an 8-bit write-only pseudo-register. The bits in this register are individually addressed by A3,A2,A1 . The data on AØ is latched into the addressed state bit by /DEV low. All eight state bits are reset to Ø by /RESET low.

Not only do the state bits control certain chip functions and outputs, the setting of two of the state bits L6 and L7, and Motor-On, internally select which register is to be selected and whether the operation is to be a read or a write. If an operation occurs that changes the state of one of these bits to a new state, that new state will select the register to be accessed during that operation and whether that operation is to be a read or a write.

Address	Name	Function
Ø		A 1 in this bit will drive PHASEØ to a high state.
1		PHASE1
2		PHASE2
3		PHASE3
4	LMotor-On	A 1 on LMotor-On sets the enable selected below low
5	Drive-Sel	A 1 on this bit selects /ENBL2; a Ø selects /ENBL1
6	L6	(see description below)
7	L7	(see description below)

The state bits L7 and L6, and Motor-On, select which register is available to be read or written. Other registers are read during any operation in which AØ is a zero. A register is written when both L6 and L7 are set or are being set to 1 and AØ is a one.

The combination of L7 and Motor-On and /underrun enables /WRREQ low.

L7	L6	Motor-On	register operation selected	State Name
Ø	Ø	Ø	read all ones	
Ø	Ø	1	read data register	Read
Ø	1	x	read status register	Write-Protect Sense
1	Ø	x	read write-handshake register	Write
1	1	Ø	write mode register	Mode Set
1	1	1	write data register	Write Load

Mode register (a write only register)

All eight mode bits are reset to Ø by /RESET low.

	bit	function
LSB	Ø	1 = latch mode (should be set in asynchronous mode)
	1	Ø = synchronous handshake protocol; 1 = asynchronous
	2	Ø = 1-second on board timer enable; 1 = timer disable
	3	Ø = slow mode; 1 = fast mode (2 uS bit cell timing)
	4	Ø = 7MHz; 1 = 8MHz (7 or 8 mHz clock descriptor)
	5	1 = test mode; Ø = normal operation
	6	1 = MT-reset
MSB	7	reserved for future expansion

In latch mode the msb of the read data is latched internally during /DEV low (this internally latched msb is then used for the determination of a valid data read).

If the 1-second timer bit is a zero then the enable (/ENBL1 or /ENBL2) selected by Drive-Sel will be held low for 2^23 +-1ØØ FCLK periods (about 1 second) after the LMotor-On state bit is reset to zero. If the latch mode bit is set the timer is not guaranteed to count up to 2^23. Motor-On is synonomous with either /ENBL1 or /ENBL2 being low.

Fast mode selects a bit cell time of 2 uS instead of 4 uS. The 7/8 mHz descriptor indicates whether the input clock (FCLK) is to be divided by 7 or 8 to provide 1 uS internal timings.

When the test mode bit is a 1, device operation is unspecified, except that status register bit 5 can always be read and that the mode register can always be set.

Status register (a read-only register)

bit	function
Ø-4	same as mode register
5	1 = either /ENBL1 or /ENBL2 is currently active (low)
6	1 = MZ (reset to Ø by /RESET and MZ-reset)
7	1 = SENSE input high; Ø = SENSE input low

The MZ bit is reserved for compatibility with future products and should always be read as a zero.

Handshake Register (a read only register)

bit	function
Ø-5	reserved for future use (currently read as ones)
6	1 = write state (cleared to Ø if a write underrun occurs)
7	1 = write data buffer register ready for data

Data Register

The operation of the data register depends on the setting of state bits L6 and L7 and on the synchronous mode bit. With L6 and L7 clear, the data register operates as a read data register. With L7 set the data register operates in the write state as a write data buffer.

Maximum Ratings
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supply voltage	-Ø.3 to +7.Ø V
input voltage	-Ø.3 to +7.Ø V
storage temperature	-35 to +125 degrees C
operating temperature	Ø to +7Ø degrees C (ambient)

DC characteristics

sym	parameter	min	max	units	notes
Vcc	supply voltage	4.75	5.25	Volts	
Icc	supply current	—	60	mA	5
Vil	Input low	—	Ø.8	V	3
Vih	Input high	2.Ø	—	V	4
Il	input leakage	—	1ØØ	uA	1
Vol	TTL output low	—	.4	V	
Voh	TTL output high	2.4	—	V	
Ioh	source current at Voh	.32	—	mA	2
Iol	sink current at Vol	3.2	—	mA	2

Notes

1. Inputs.

   The inputs have static protection. All IWM inputs and bidirectional lines in the input mode are high impedance except as noted below:

   WPROT and /RDDATA : pullup to VCC of 1ØK ohms nominal
   (source current of 8Ø to 6ØØ uA at Ø Volts with VCC = 5.25V

2. Outputs Ioh and Iol apply to DØ thru D7 and WRDATA. The following output lines have special drive capabilities, noted below.

   /ENBL1, /ENBL2: Sink current of at least 5.Ø mA at Vol
   Source current of at least 4Ø uA at Voh

   /WRREQ: Sink current of at least 1Ø.Ø mA at Vol
   Source current of at least 4Ø uA at Voh

   PHASE 0, PHASE 2 Source current of at least 1.Ø mA at Voh
   PHASE 3 Source current of Ø.5 mA when pulled down to 3.Ø V.
   Sink current of at least 2.4 mA at Vol

   PHASE 1: Source current of at least 1.0 mA at Voh
   Source current of 0.5 mA when pulled down to 3.0V
   Sink current of at least 12.4 mA at Vol

3. TTL Vil is also referred to as a zero.

4. TTL Vih is also referred to as a one.

5. At 5.25 V over full operating temperature range.

AC characteristics

sym	parameter	min	max	units	notes
tas	A0-A3 to /DEV, fe	40	—	nS	setup
tah	/DEV, re to A0-A3 invalid	-1		nS	addr hold
tds	data to (Q3 OR /DEV), re	50	—	nS	setup
tdh	(Q3 OR /DEV), re to data	10	—	nS	data hold
tda	/DEV, fe to data out	—	100	nS	access, 1.
tdsl	/DEV low	200	—	nS	6.
tdsh	/DEV high	450	—	nS	
tde	/DEV to /ENBLx or /WRREQ	—	60	nS	2.
tdph	/DEV to PHASEx	—	60	nS	2.
trdh	RDDATA high time	300	—	nS	5.
tckh	FCLK high time	50	200	nS	At 8MHZ
tckl	FCLK low time	50	200	nS	At 8MHZ
tckp	FCLK period, with timer	120	143	nS	
tckpt	FCLK period, no timer	120	500	nS	11.
tqdsl	Q3, re to /DEV, fe	1	200	nS	7.
tqdsh	Q3, re to /DEV, re	1	200	ns	7.
tq3h	Q3 high	260	300	nS	7.
tq3l	Q3 low	190	—	nS	7.
tdmsbh	D0-6 valid to D7 re	50	—	nS	8.
tres	/RESET low time	500	—	nS	10.
trwrh	/RESET to /WRREQ high	—	300	nS	
tsj	sampling jitter	—	10	nS	4.
tckwr	write clock, re to WRDATA	—	500	nS	9.
twrj	write data jitter	—	15	nS	9.
cp	input pin capacitance	—	15	pF	

notes

1. Load = 130 pF and 8 LS TTL loads
2. Load = 100 pf and rated maximum current
3. fe = falling edge (TTL high to low)
   re = rising edge
4. tsj is the uncertainty window in sampling the asynchronous input RDDATA and synchronizing it internally with CLK at any constant Vcc and temperature.
5. trdh and trdl must be at least twice the period of CLK to be properly synchronized.
6. the time between 2 succesive /DEV selects will be greater than 2 CLK periods, and in synchronous mode will be no less than 1 Q3 period. /DEV may be held low indefinitly.
7. These apply to the synchonous mode only. In other modes Q3 may be held low indefinitly.
8. If, when /DEV is low, data on D0-7 is changing to a word with D7 high, the data on D0-6 must become valid before the rising edge of D7 .
9. tckwr is the time from FCLK, re, in asynchronous mode, or Q3, re, in synchronous mode, to changes in the output WRDATA, driving a load of 100 pF.
   twrj is the change in tckwr from edge to edge of WRDATA at any constant Vcc and temperature.
10. for test purposes tres must be at least 24 times tckp .
11. tckpt is max FCLK period with 1-second timer disabled.

This specification is confidential to Apple and contains proprietary information.

changes from earlier specs

A0-3 pinout corrected
/ENBL1 and /ENBL2 pinout corrected
tdmsbh specified
latch mode added (change to breadboard also)

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changes from rev#11 spec (4/16/82)

D0-7 pinout changed to facilitate IC layout
write jitter specified

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changes from rev#12 spec (5/5/82)

Address setup time changed to 40 nS

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changes from rev#14 spec (6/4/82)

LMotor-On different from Motor-On
Phase lines sink 2.4 mA
tres test condition added
underrun and other nomenclatured cleared up

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changes from rev#17 spec (8/17/82)
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read data stall time changed to 4 CLKs
relaxed AC and DC characteristics

rhn 02/05/82
bcs 01/11/82
ws 10/20/81
woz 1978,79