The ATM Forum

Technical Committee

# Interoperability Abstract Test Suites for the Physical Layer

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**Interoperability Abstract Test Suites for the Physical Layer**

Version 1.0

April, 1995

# Table of Contents

# 1. Introduction

This document presents a set of interoperability test suites for the Physical layer. It belongs to a set of test documents supplied by the ATM Forum that cover the testing areas conformance, performance and interoperability testing. The document "Introduction to ATM Forum Test Specification" [2] provides an introduction to the different testing areas and should be consulted prior to using this test suite.

## 1.1 Scope

This document presents a set of interoperability test suites for the Physical layer. Included in this set are test cases that address:

- DS3 physical layer
- STS-3c physical layer
- 100 Mbps multimode fibre physical layer.

It includes sample test cases that address interoperability at different levels. These levels include:

- Basic Connectivity: These tests are applied when both SUTs meet or claim conformance to the ATM Forum UNI specifications [1]. Some of these tests may be eliminated if thorough dynamic conformance testing has taken place and the results have been analyzed prior to interoperability testing.
- Support of Optional Features/Functions: These tests are applied when one or both of the SUTs support a feature or function that is specified as an option. They are not applied when neither of the SUTs support that feature or function.

If one or both of the SUTs support a proprietary feature, additional test cases will be required to address its effect on interoperability. These test cases can be added as required but are not part of these test suites.

Systems under test (SUTs) are ATM network elements (e.g. ATM switches, multiplexers etc.) connected via UNI as defined in [1] section 1.6. The network management messages to control functions within the physical layer are not part of this document.

## 1.1 References

[1] ATM User-Network Interface Specification, Version 3.0, ATM Forum, September 1993.

[2] Introduction to ATM Forum Test Specifications, ATM Forum, AF-TEST-0022.000, November 1994

## 1.2 Abbreviations

| | |
|---|---|
| AIS | Alarm Indication Signal |
| ATM | Asynchronous Transfer Mode |
| ATS | Abstract Test Suite |
| BER | Bit Error Ratio |
| BIP-8 | Bit Interleaved Parity (byte wide) |
| CLP | Cell Loss Priority |
| FEBE | Far End Block Error |
| FERF | Far End Receive Failure |
| GFC | Generic Flow Control |
| IOP | Interoperability |
| LOS | Loss Of Signal |
| PLCP | Physical Layer Convergence Protocol |
| PMD | Physical Media Dependent |
| PT | Payload Type |
| QoS | Quality of Service |
| SUT | System Under Test |
| TC | Transmission Convergence |
| VC | Virtual Channel |
| VCC | Virtual Channel Connection |
| VCI | Virtual Channel Identifier |
| VP | Virtual Path |
| VPC | Virtual Path Connection |
| VPI | Virtual Path Identifier |

# 2. Test Realization

The realization of each test case within this test suite shall be the responsibility of test realizer or the test laboratory. The test realization shall adhere to the following condition:

- the realization of a test case shall meet all of the requirements and objectives of the test case as specified in the test purpose.

# 3. Test Configuration

The general test setups for IOP tests between two ATM switches are shown in the following figures. Only the relevant components are illustrated.

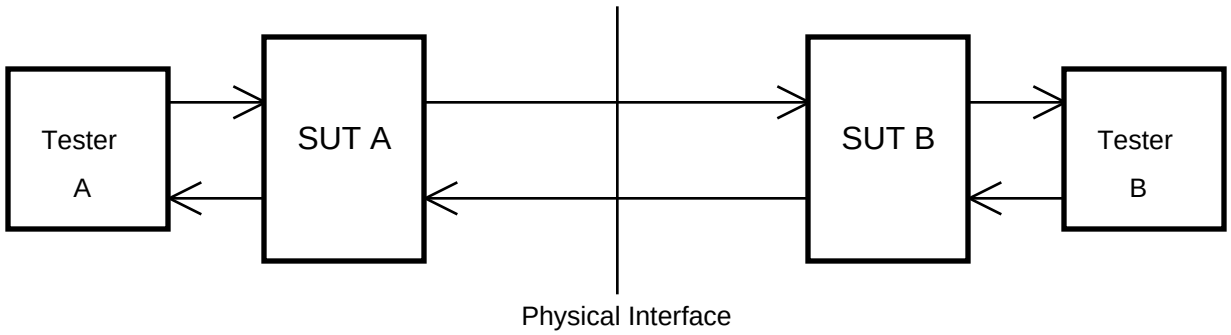


Figure 3.1: Test Configuration #1

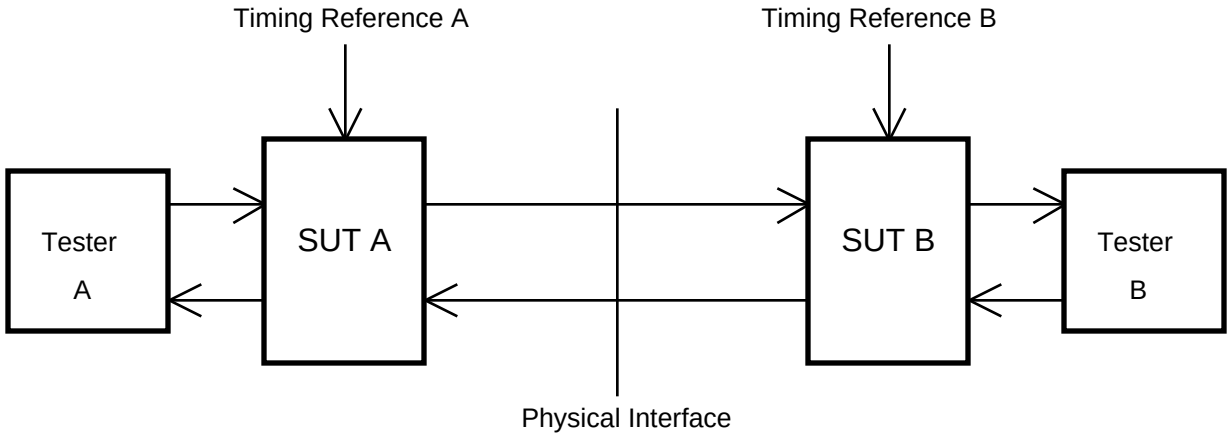


Figure 3.2: Test Configuration #2

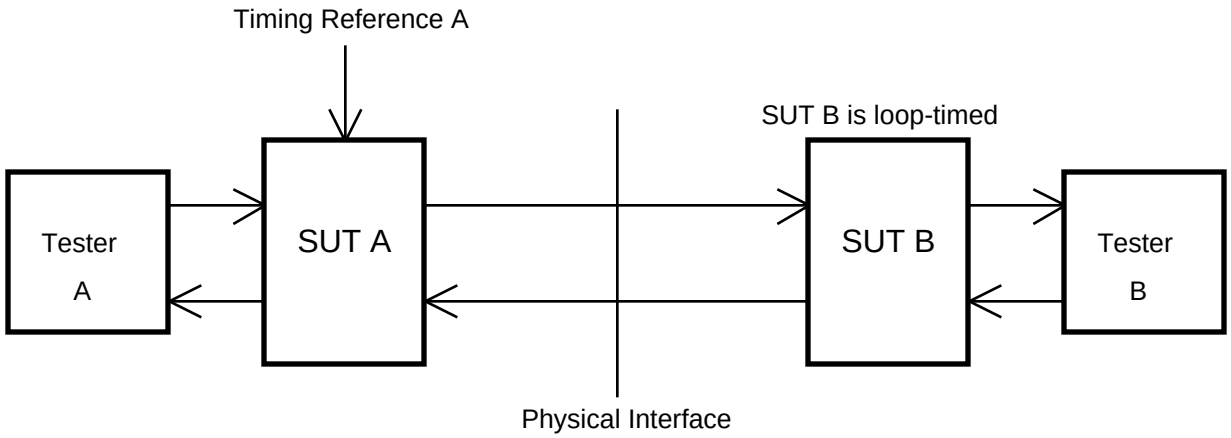


Figure 3.3: Test Configuration #3

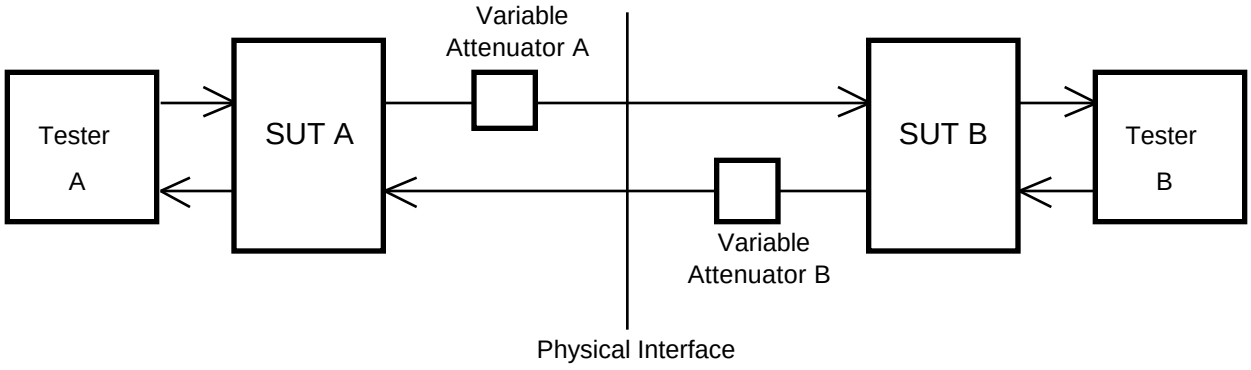


Figure 3.4: Test Configuration #4

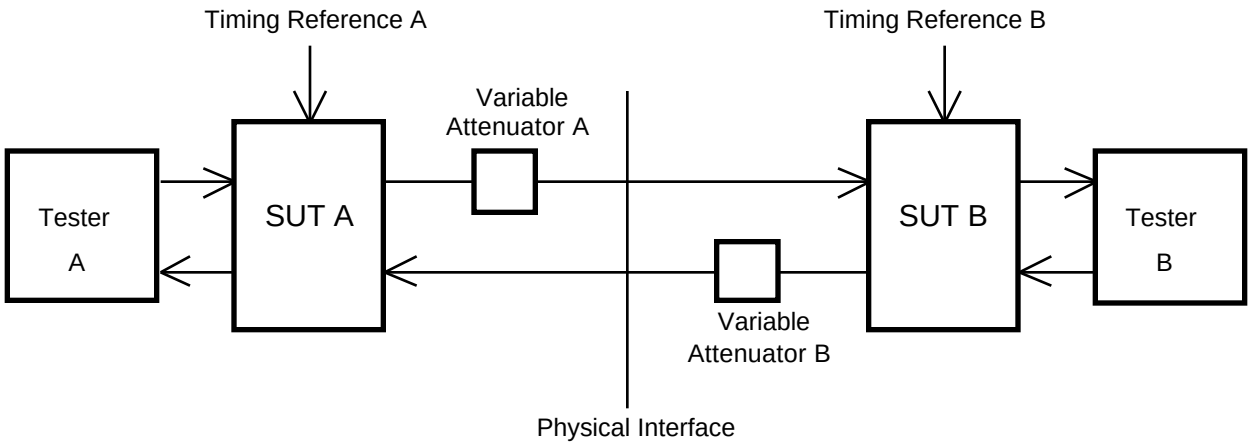


Figure 3.5: Test Configuration #5

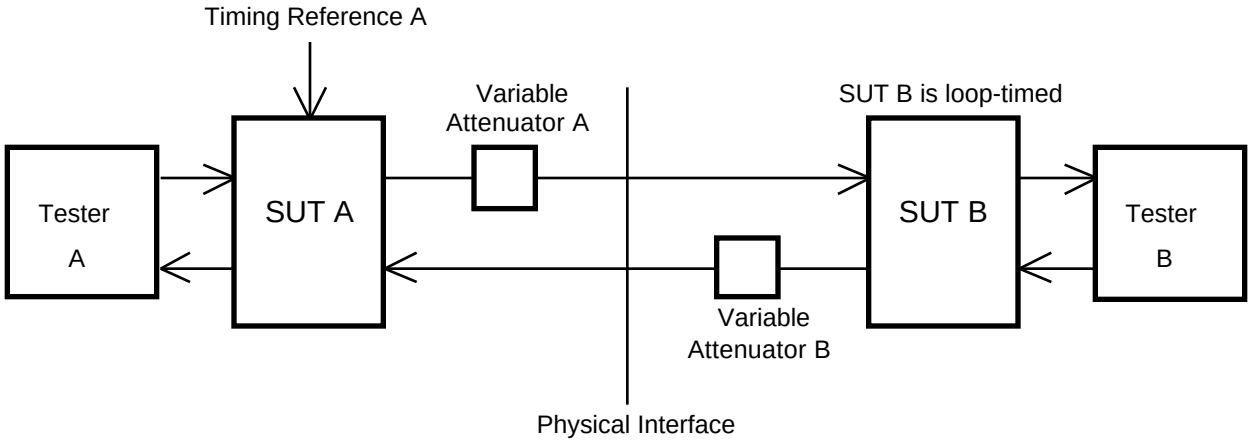


Figure 3.6: Test Configuration #6

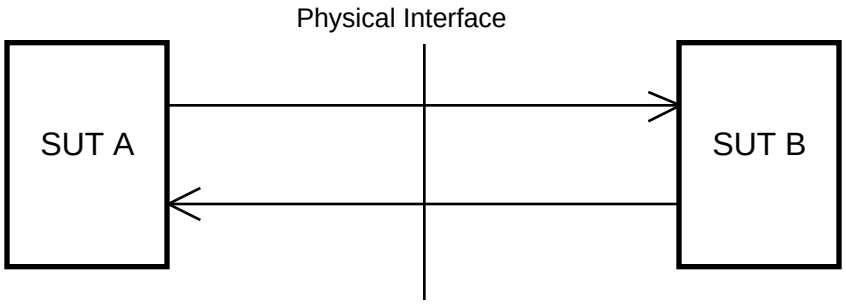


Figure 3.7: Test Configuration #7

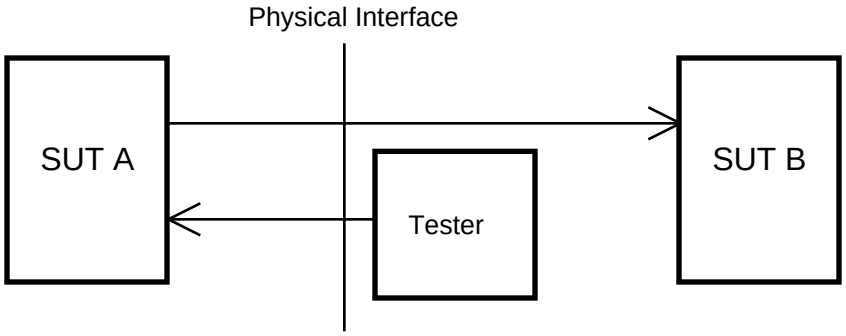


Figure 3.8: Test Configuration #8

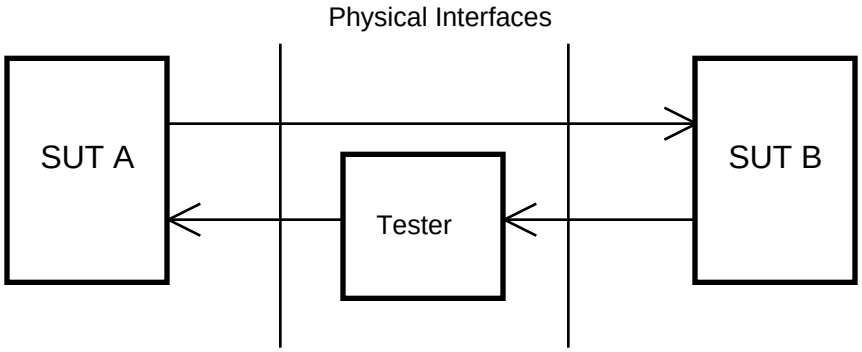


Figure 3.9: Test Configuration #9

# 4. DS3 Physical Layer Test Suite

## 4.1 Test Case Index

| No | Test Case ID | Test case name | UNI 3.0 Reference | Test Config. # |
|---|---|---|---|---|
| 1 | DS3/LOS/1 | Recovery from loss of signal (LOS) | none | 7 |
| 2 | DS3/PMD/1 | Electrical signal performance with minimum and maximum cable lengths | 2.2.1 | 1 |
| 3 | DS3/TC/1 | Performance under external timing failure conditions - external timing | 2.2.3 | 2 |
| 4 | DS3/TC/2 | Performance under external timing failure conditions - loop timing | 2.2.3 | 3 |
| 5 | DS3/TC/3 | Performance under loop timing failure conditions | 2.2.3 | 3 |
| 6 | DS3/CBIT/1 | C-bit parity error test | 2.2.1 | 7 |
| 7 | DS3/CBIT/2 | C-bit parity interoperability test | 2.2.1 | 7 |
| 8 | DS3/CBIT/3 | C-bit Far End Block Errors (FEBE) | 2.2.1.2.4 | 8 |
| 9 | DS3/PLCP/1 | PLCP framing and nibble stuffing test | 2.2.1.1 | 7 |
| 10 | DS3/PMD/2 | PLCP Remote Alarm Indication (RAI) | 2.2.1.2.4 | 7 |
| 11 | DS3/B8/1 | BIP-8 error test | 2.2.1.2.2 | 7 |
| 12 | DS3/B8/2 | BIP-8 interoperability test | 2.2.1.2.2 | 7 |
| 13 | DS3/PS/1 | Cell payload scrambling interoperability test | 2.2.4 | 1 |
| 14 | DS3/PS/2 | Unscrambled cell payload interoperability test | 2.2.4 | 1 |
| 15 | DS3/HEC/1 | HEC interoperability test | 2.2.6 | 1 |

## 4.2 Test Cases Dynamic Behavior

**1. Test Case ID: DS3/LOS/1**

Test Case Name: Recovery from loss of signal (LOS).
Test Purpose: To verify the recovery of signal levels, line coding, line rates, and bit timing when the SUTs operate in the free running mode.
Pre-requisite: Always run.
Reference: none
Test Configuration: #7

Test Set-up:
1. Configure both SUTs to operate in the C-bit parity mode.
2. Configure both SUTs to transmit information using their local timing sources.

Test Procedure:

1. Break the physical links connecting the two SUTs.
2. Ensure that both SUTs acknowledge that the incoming signal is lost.
3. Reconnect the two SUTs. Observe that Physical Layer Convergence Protocol (PLCP) frame synchronization is restored.
4. Observe that all alarms raised when the links were broken are cleared when the link is reconnected.

Verdict Criteria:

PLCP frame synchronization shall be restored and all the alarms raised after the link is broken shall be cleared automatically after the physical link between the two SUTs is reestablished. In addition, all error counters that were being incremented because of the broken link shall cease to increment once the physical link is re-established.

**2. Test Case ID: DS3/PMD/1**

| | |
|---|---|
| Test Case Name: | Electrical signal performance with minimum and maximum cable lengths. |
| Test Purpose: | This test is intended to determine a cable length range where the connected SUTs can operate properly (bit and clock recovery). |
| Pre-requisite: | Always run. |
| Reference: | [1], Section 2.2.1 |
| Test Configuration: | #1 |

Test Set-up:

1. Configure the system so that traffic originated by Tester A is passing over the DS3 physical interface between SUT A and B to Tester B.
2. Tester B monitors the received traffic.

Test Procedure:

1. Adjust the Line Buildout (LBO) at SUT A's transmitter for the minimum length of cable (i.e., 0 feet), and make cable length to the receiver side of SUT B as short as possible.
2. Check the DS3 Performance Monitoring registers at SUT B for coding violations. If this function is not available or accessible, the performance monitoring of PLCP B1, received cell rate, cell error rate or BER of the ATM payload can be used.
3. Repeat Steps 1 and 2, with the LBO set for the maximum length of cable (i.e., 450 feet), and make cable length to the transmitter side of SUT A and the receiver side of SUT B equal to 450 feet each (i.e., 900 feet total).
4. Repeat the test set-up and procedure with the roles of SUT A and SUT B reversed.
5. Repeat Steps 1 to 4 with transmitter signal loaded with maximum jitter/wander.

Verdict Criteria:

The code violation error rate must be better than $10^{-9}$ in all cases and no physical layer alarms associated with the received signal level shall be raised.

**3. Test Case ID: DS3/TC/1**

| | |
|---|---|
| Test Case Name: | Performance under external timing failure conditions - external timing. |
| Test Purpose: | This test is intended to verify that both SUTs will perform properly over all frequencies of the free-running modes of both SUTs. |
| Pre-requisite: | Both SUTs are capable of being timed using signals other than the PLCP frame rate received from the other SUT (e.g., external DS1 timing, line-timing using the PLCP frame rate from a different source). |
| Reference: | [1], Section 2.2.3 |
| Test Configuration: | #2 |

Test Set-up:

1. Configure the system so that traffic originated by Tester A is passing over the DS3 physical interface between SUT A and B to Tester B and vice versa.
2. Testers A and B monitor the received traffic.

Test Procedure:

1. Configure Testers A and B to generate cell traffic on the DS3 physical interface in both directions at approximately 90% of the maximum cell rate that can be transported. Make sure the system is operating error-free.
2. Adjust the frequencies of Timing References A and B so that the PLCP frame rates in the DS3 signals transmitted by SUT A and SUT B are the worst-case rates (SUT A at the minimum and SUT B at the maximum rate or vice versa) that could occur if SUT A and SUT B were free-running (based on the SUTs' internal clock accuracy specifications). Note if any bit errors or traffic interruptions occur.
3. If bit errors or traffic interruptions occur, adjust the Timing Reference frequencies to determine the combinations of offsets that cause errors.

Verdict Criteria:

The received traffic shall be error-free and no physical layer alarms shall be raised for all timing reference frequencies.

### 4. Test Case ID: DS3/TC/2

| | |
|---|---|
| Test Case Name: | Performance under external timing failure conditions - loop timing. |
| Test Purpose: | This test is intended to verify that both SUTs are able to loop the recovered timing over all frequencies of the free-running modes of both SUTs. |
| Pre-requisite: | One SUT (designated SUT A) is capable of being timed using a signal from an external source (e.g., external DS1 timing, or line timing using the PLCP frame rate in a signal from a source other than the other SUT), and the other SUT is capable of being loop-timed. |
| Reference: | [1], Section 2.2.3 |
| Test Configuration: | #3 |

Test Set-up:

1. Configure the system so that traffic originated by Tester A is passing over the DS3 physical interface between SUT A and B to Tester B and vice versa.
2. Testers A and B monitor the received traffic.

Test Procedure:

1. Configure Testers A and B to generate cell traffic on the DS3 physical interface in both directions at approximately 90% of the maximum cell rate that can be transported. Make sure the system is operating error-free.
2. Adjust the frequency of Timing Reference A so that the PLCP frame rate in the DS3 signal transmitted by SUT A is the worst-case rate that could occur if SUT A were free-running (based on SUT A's internal clock accuracy specifications). Note if any bit errors or traffic interruptions occur.
3. If bit errors or traffic interruptions occur, adjust the Timing Reference frequencies to determine the combinations of offsets that cause errors.
4. If SUT A can be loop-timed and SUT B can be timed using a signal from an external source, then repeat the test set-up and procedure with the roles of SUT A and SUT B reversed.

Verdict Criteria:

The received traffic shall be error-free and no physical layer alarms shall be raised for all timing reference frequencies.

**5. Test Case ID: DS3/TC/3**

Test Case Name: Performance under loop timing failure conditions.
Test Purpose: This test is intended to verify that the signal transmitted by a loop-timed SUT can be received by the other SUT when the reference signal fails.
Pre-requisite: One or both of the SUTs are capable of being loop-timed.
Reference: [1], Section 2.2.3
Test Configuration: #3

Test Set-up:

1. Configure the system so that traffic originated by Tester A is passing over the DS3 physical interface between SUT A and B to Tester B and vice versa.
2. Time SUT A using a reference signal from an external source, or allow it to free run. Loop time SUT B.
3. Testers A and B monitor the received traffic.

Test Procedure:

1. Configure Testers A and B to generate cell traffic on the DS3 physical interface in both directions at approximately 90% of the maximum cell rate that can be transported. Make sure the system is operating error-free.
2. Cause an LOS at SUT B's receiver.
3. Check the Tester A at SUT A for the Bit Error Ratio (BER), received cell rate, and cell error rate. Also check the DS3 and PLCP B1 Performance Monitoring registers at SUT B for coding violations.
4. If SUT A can be loop-timed, then repeat the test set-up and procedure with the roles of SUT A and SUT B reversed.

Verdict Criteria:

The received traffic in one direction of transmission shall still be error-free when there is an LOS in the other direction.

**6. Test Case ID: DS3/CBIT/1**

Test Case Name: C-bit parity error test.
Test Purpose: To verify that both SUTs A and B detect C-bit parity errors.
Pre-requisite: Conditional on C-bit parity implementation.
Reference: [1], Section 2.2.1
Test Configuration: #7

Test Set-up:

1. Establish a connection between the physical transmit and receive ports of SUT A.
2. Configure the SUT to operate in the C-bit parity mode.

Test Procedure:

1. Use the SUT B (SUT B can be replaced by test equipment) to cause C-bit parity errors on the DS3 link to the SUT A.
2. Substitute SUT A with SUT B and repeat the experiment.

Verdict Criteria:

Both SUTs shall detect the C-bit parity errors.

**7. Test Case ID: DS3/CBIT/2**

Test Case Name: C-bit parity interoperability test.
Test Purpose: To verify interoperability in the computation of the C-bit parity.
Pre-requisite: Conditional on successful completion of DS3/CBIT/1.
Reference: [1], Section 2.2.1

Test Configuration: #7

Test Set-up:
1. Connect the physical link between the two SUTs.
2. Configure both SUTs to operate in the C-bit parity mode.

Test Procedure:
1. Observe the C-bit parity error indicator on both SUTs.

Verdict Criteria:
This test is passed if both SUTs raise no C-bit parity errors.

**8. Test Case ID: DS3/CBIT/3**

Test Case Name: C-bit Far End Block Errors (FEBE).
Test Purpose: To verify interoperability in the C-bit FEBE field.
Pre-requisite: Conditional on successful completion of DS3/CBIT/1.
Reference: [1], Section 2.2.1.2.4
Test Configuration: #8

Test Set-up:
1. Configure both SUTs to operate in the C-bit parity mode.

Test Procedure:
1. Use the tester to cause C-bit parity errors on the DS3 link to SUT A.
2. Observe that SUT A declares C-bit parity errors.
3. Observe that SUT B detects and declares the same number of C-bit FEBEs.
4. Repeat this test with the relative positions of SUTs A and B interchanged.

Verdict Criteria:
Both SUTs shall recognize the FEBEs sent by the other SUT.

**9. Test Case ID: DS3/PLCP/1**

Test Case Name: PLCP framing and nibble stuffing test.
Test Purpose: To verify interoperability in PLCP framing octet and stuffing cycle.
Pre-requisite: Always run.
Reference: [1], Section 2.2.1.1
Test Configuration: #7

Test Set-up:
1. Configure both SUTs to operate in the C-bit parity mode.

Test Procedure:
1. Observe that the two SUTs clear their respective Loss Of PLCP Frame alarms.
2. The ability to achieve PLCP frame synchronization would indicate interoperability in PLCP framing octets, C1 octet, and the nibble stuffing cycles.

Verdict Criteria:
The two SUTs shall acquire PLCP framing synchronization.

**10. Test Case ID: DS3/PMD/2**

Test Case Name: PLCP Remote Alarm Indication (RAI).
Test Purpose: To verify interoperability in the PLCP RAI bit.
Pre-requisite: Always run.
Reference: [1], Section 2.2.1.2.4

Test Configuration: #7

Test Set-up:
1. Configure both SUTs to operate in the C-bit parity mode.

Test Procedure:
1. Break the physical link connecting the transmit port of SUT B to the receive port of SUT A.
2. Observe that SUT A declares a DS3 Loss Of Signal (LOS) or red alarm.
3. Observe that SUT B detects the PLCP Remote Alarm Indication (RAI) bit sent by SUT A and declares a yellow alarm.
4. Repeat this test with the relative positions of SUTs A and B interchanged.

Verdict Criteria:
Both SUTs shall recognize the PLCP RAI sent by the other SUT.

### 11. Test Case ID: DS3/B8/1

Test Case Name: BIP-8 error test.
Test Purpose: To verify that both SUTs A and B detect BIP-8 errors.
Pre-requisite: Always run.
Reference: [1], Section 2.2.1.2.2
Test Configuration: #7

Test Set-up:
1. Establish a connection between the physical receive and transmit ports of SUT A.
2. Configure the SUT to operate in the C-bit parity mode.

Test Procedure:
1. Use the SUT B (SUT B can be replaced by test equipment) to cause BIP-8 errors on the DS3 link to the SUT A.
2. Observe that SUT A detects and indicates BIP-8 errors.
3. Substitute SUT A for SUT B and repeat the experiment.

Verdict Criteria:
Both SUTs shall be able to detect the BIP-8 errors.

### 12. Test Case ID: DS3/B8/2

Test Case Name: BIP-8 interoperability test.
Test Purpose: To verify interoperability in BIP-8 calculations.
Pre-requisite: Conditional on the successful completion of DS3/B8/2.
Reference: [1], Section 2.2.1.2.2
Test Configuration: #7

Test Set-up:
1. Configure both SUTs to operate in the C-bit parity mode.

Test Procedure:
1. Observe the BIP-8 error counters on both SUTs.

Verdict Criteria:
The computation of BIP-8 is compatible if both SUTs do not detect and indicate any BIP-8 errors.

### 13. Test Case ID: DS3/PS/1

Test Case Name: Cell payload scrambling interoperability test.
Test Purpose: To verify interoperability when cell payload scrambling is enabled.
Pre-requisite: Always run.

Reference: [1], Section 2.2.4
Test Configuration: #1

Test Set-up:
1. Configure both SUTs to operate in the C-bit parity mode.
2. Activate cell scrambling on both SUTs.
3. Establish appropriate connections on both SUTs to pass bi-directional traffic between SUTs A and B.
4. Configure the cell generators of the two testers to generate cells at 90% of the maximum data rate.

Test Procedure:
1. Observe that the testers are able to receive scrambled cells without any corruption in the payload of the ATM cells.

Verdict Criteria:
SUTs A and B shall be able to send and receive scrambled ATM cells in both directions.

### 14. Test Case ID: DS3/PS/2

Test Case Name: Unscrambled cell payload interoperability test.
Test Purpose: To verify interoperability when cell payload scrambling is disabled.
Pre-requisite: Always run.
Reference: [1], Section 2.2.4
Test Configuration: #1

Test Set-up:
1. Configure both SUTs to operate in the C-bit parity mode.
2. Deactivate cell scrambling on both SUTs.
3. Establish appropriate connections on both SUTs to pass bi-directional traffic between SUTs A and B.
4. Configure the two testers to generate cells at 90% of the maximum data rate.

Test Procedure:
1. Observe that the testers are able to receive unscrambled cells without any corruption in the payload of the ATM cells.

Verdict Criteria:
SUTs A and B shall be able to send and receive unscrambled ATM cells in both directions.

### 15. Test Case ID: DS3/HEC/1

Test Case Name: HEC interoperability test.
Test Purpose: To verify interoperability in HEC calculations.
Pre-requisite: Always run.
Reference: [1], Section 2.2.6
Test Configuration: #1

Test Set-up:
1. Establish appropriate connections on both SUTs to pass uni-directional traffic from SUT A to SUT B.
2. Configure the Tester A to generate cells at 90% of the date rate with the GFI field set to 0.

Test Procedure:
1. Use the Tester A to generate cells from SUT A to SUT B.
2. Verify that no cells are dropped.
3. Verify also that SUT B does not raise any HEC errors on the cells generated by SUT A.
4. Repeat this test with the relative positions of SUTs A and B interchanged.

Verdict Criteria:

The calculation of HEC is interoperable if no cells are dropped and no HEC errors are encountered by both SUTs.

# 5. STS-3c Physical Layer Test Suite

## 5.1 Test Case Index

| No. | Test Case ID | Test case name | UNI 3.0 Reference | Test Config. # |
|---|---|---|---|---|
| 1 | STS3C/LOS/1 | Recovery from loss of signal | none | 7 |
| 2 | STS3C/PMD/1 | Minimum and maximum optical attenuation performance | 2.1.1.1.1 | 4 |
| 3 | STS3C/PMD/2 | Performance in the presence of dispersion | 2.1.1.1.1 | 4 |
| 4 | STS3C/FMG/1 | Interoperability for SONET STS-3c framing | 2.1.1.2.1 | 7 |
| 5 | STS3C/TC/1 | Performance under external timing failure conditions - external timing | 2.1.1.2.1 | 5 |
| 6 | STS3C/TC/2 | Performance under external timing failure conditions - loop timing | 2.1.1.2.1 | 6 |
| 7 | STS3C/TC/3 | Performance under loop timing failure conditions | 2.1.1.2.1 | 6 |
| 8 | STS3C/OH/1 | Interoperability for SONET section overhead generation and processing - I | 2.1.1.2.1/ 2.1.2.1.1 | 7 |
| 9 | STS3C/OH/2 | Interoperability for SONET section overhead generation and processing - II | 2.1.1.2.1 | 7 |
| 10 | STS3C/OH/3 | Interoperability for line layer overhead generation and processing - I | 2.1.1.2.1/ 2.1.2.1.1 | 7 |
| 11 | STS3C/OH/4 | Interoperability for line layer overhead generation and processing - II | 2.1.1.2.1 | 7 |
| 12 | STS3C/OH/5 | Interoperability for line layer overhead generation and processing - III | 2.1.1.2.1/ 2.1.2.1.1 | 8 |
| 13 | STS3C/OH/6 | Interoperability for path layer overhead generation and processing - I | 2.1.1.2.1/ 2.1.2.1.1 | 7 |
| 14 | STS3C/OH/7 | Interoperability for path layer overhead generation and processing - II | 2.1.1.2.1 | 7 |
| 15 | STS3C/OH/8 | Interoperability for path layer overhead generation and processing - III | 2.1.1.2.1/ 2.1.2.1.1 | 8 |
| 16 | STS3C/PS/1 | Interoperability for B-ISDN specific TC sublayer functions - I | 2.1.1.2.2.2 | 4 |
| 17 | STS3C/CDL/1 | Interoperability for B-ISDN specific TC sublayer functions - II | 2.1.1.2.2.3/ 2.1.1.2.2.4 | 4 |
| 18 | STS3C/HEC/1 | HEC interoperability test | 2.1.1.2.2.1 | 4 |

## 5.2 Test Cases Dynamic Behavior

**1. Test Case ID: STS3C/LOS/1**

Test Case Name: Recovery from loss of signal.
Test Purpose: To verify recovery for signal levels, line rate and bit timing when the SUTs operate in the free-running mode.
Pre-requisite: Always run.
Reference: none
Test Configuration: #7

Test Set-up:
1. Configure SUT A and SUT B in the free running mode of operation.

Test Procedure:
1. Break the physical link connecting the two SUTs.
2. Verify that the receiver on each SUT indicates a loss of signal.
3. Reconnect the SUTs again.
4. Observe that the receiver on each SUT reestablishes synchronization to the incoming line signal.
5. In the above test, note the following information: alarms and error statistics at the Physical Layer (Section, Line and Path) as gathered by each of the SUTs. Typical alarms include: SONET Physical Performance Monitoring values invalid, SONET Section loss of frame, SONET Line AIS and FERF, SONET Path AIS, SONET Path loss of pointer, etc. Typical statistics (error counters) include: errored seconds, severely errored seconds, unavailable seconds, etc.

Verdict Criteria:
Complete recovery from the loss of signal is necessary. This includes all generated alarms during the loss of signal are cleared and error counters stop increasing.

**2. Test Case ID: STS3C/PMD/1**

Test Case Name: Minimum and maximum optical attenuation performance.
Test Purpose: This test is intended to verify that the SUTs operate properly with the minimum and maximum amount of optical attenuation between their transmitters and receivers.
Pre-requisite: Always run.
Reference: [1], Section 2.1.1.1.1
Test Configuration: #4

Test Set-up:
1. Configure the system so that traffic originated by Tester A is received by SUT A, multiplexed or switched to the STS-3c signal transmitted to SUT B, demultiplexed or switched at SUT B, and transmitted to Tester B.

Test Procedure:
1. Adjust Variable Attenuator B so that the optical power level of the STS-3c signal received by SUT A is within the receiver's specified range (e.g., in the middle of its range).
2. Adjust Variable Attenuator A so that the optical signal power at SUT B's receiver is the maximum specification of SUT B.
3. Insert traffic at SUT A at a rate at approximately 90% of the maximum rate that can be transported.
4. Check the Tester B at SUT B for the BER of the ATM cell payload, received cell rate, and cell error rate. Also check the SONET Performance Monitoring registers at SUT B for B1, B2 and B3 coding violations. Record the BER of the ATM cell payload.
5. Adjust Variable Attenuator A so that the optical signal power at SUT B's receiver is the minimum specification of SUT B.

6. Check the Tester B at SUT B for the BER, received cell rate, and cell error rate. Also check the SONET Performance Monitoring registers at SUT B for B1, B2 and B3 coding violations. Record the BER.
7. Repeat the test set-up and procedure with the roles of SUT A and SUT B reversed.

Verdict Criteria:
The measured BER must be better than $10^{-10}$ in all cases, and no physical layer alarms associated with the received signal level are detected.

### 3. Test Case ID: STS3C/PMD/2

Test Case Name: Performance in the presence of dispersion.
Test Purpose: This test is intended to verify that the SUTs operate properly with the maximum amount of optical dispersion and attenuation between their transmitters and receivers.
Pre-requisite: One or both of the SUTs use MLM transmitters.
Reference: [1], Section 2.1.1.1.1
Test Configuration: #4

Test Set-up:
1. If SUT A uses an MLM transmitter, configure the system so that traffic originated by Tester A is received by SUT A, multiplexed or switched to the STS-3c signal transmitted to SUT B, demultiplexed or switched at SUT B, and transmitted to Tester B.

Test Procedure:
1. Adjust Variable Attenuator B so that the optical power level of the STS-3c signal received by SUT A is within the receiver's specified range (e.g., in the middle of its range).
2. From the dispersion coefficient of the available fiber, the maximum dispersion and spectral width specifications, and the measured spectral width of SUT A's transmitter, calculate the length of fiber that will result in the specified pulse broadening value.
3. Insert the calculated length of fiber between Variable Attenuator A and SUT B's receiver.
4. Adjust Variable Attenuator A so that the optical signal power at SUT B's receiver is the minimum of SUT B's specification.
5. Insert traffic at SUT A at a rate at approximately 90% of the maximum rate that can be transported.
6. Check the tester at SUT B for the BER of the ATM cell payload, received cell rate, and cell error rate. Also check the SONET Performance Monitoring registers at SUT B for B1, B2 and B3 coding violations. Record the BER of the ATM cell payload.
7. If SUT B uses an MLM transmitter, then repeat the test set-up and procedure with the roles of SUT A and SUT B reversed.

Verdict Criteria:
The measured BER must be better than $10^{-10}$ in all cases and no physical layer alarms are raised.

### 4. Test Case ID: STS3C/FMG/1

Test Case Name: Interoperability for SONET STS-3c framing.
Test Purpose: To verify interoperability for STS-3c framing.
Pre-requisite: Always run.
Reference: [1], Section 2.1.1.2.1
Test Configuration: #7

Test Set-up:
1. Connect the physical link between SUT A and SUT B.

Test Procedure:

1. Observe that the receivers on both SUTs are able to frame to the incoming data stream. This is an indication that the SONET Section layers on both SUTs are able to perform frame and octet boundary detection and alignment, based on the detection of the framing pattern in bytes A1 and A2.
2. Check for the SONET Section Loss of Frame alarm.

Verdict Criteria:

The two SUTs should be able to frame to the incoming data stream. No SONET Section Loss of Frame should be detected.

### 5. Test Case ID: STS3C/TC/1

| | |
|---|---|
| Test Case Name: | Performance under external timing failure conditions - external timing. |
| Test Purpose: | This test is intended to verify that both SUTs will perform properly over all frequencies of the free-running modes of both SUTs. |
| Pre-requisite: | Both SUTs are capable of being timed using signals other than the STS-3c signal received from the other SUT (e.g., external DS1 timing, or line-timing using an STS-3c from a different source). |
| Reference: | [1], Section 2.1.1.2.1 |
| Test Configuration: | #5 |

Test Set-up:

1. Configure the system so that traffic originated by Tester A(B) is received by SUT A (B), multiplexed or switched to the STS-3c signal transmitted to SUT B (A), demultiplexed or switched at SUT B (A), and transmitted to Tester B (A).

Test Procedure:

1. Insert traffic at SUTs A and B at rates at approximately 90% of the maximum rate that can be transported, and adjust the attenuators so that the system is operating error-free.
2. Adjust the frequencies of Timing References A and B so that the bit rates of the STS-3c signals transmitted by SUT A and SUT B are the worst-case rates that could occur if SUT A and SUT B were free-running (based on the SUTs' internal clock accuracy specifications). Note if any bit errors or traffic interruptions occur.
3. If bit errors or traffic interruptions occur, adjust the Timing Reference frequencies to determine the combinations of offsets that cause errors.

Verdict Criteria:

The traffic should be error-free for all timing reference frequencies.

### 6. Test Case ID: STS3C/TC/2

| | |
|---|---|
| Test Case Name: | Performance under external timing failure conditions - loop timing. |
| Test Purpose: | This test is intended to verify that both SUTs are able to loop the recovered timing over all frequencies of the free-running modes of both SUTs. |
| Pre-requisite: | One SUT (designated SUT A) is capable of being timed using a signal from an external source (e.g., external DS1 timing, or line timing using an STS-3c signal from a source other than the other SUT), and the other SUT is capable of being loop-timed. |
| Reference: | [1], Section 2.1.1.2.1 |
| Test Configuration: | #6 |

Test Set-up:

1. Configure the system so that traffic originated by Tester A(B) is received by SUT A (B), multiplexed or switched to the STS-3c signal transmitted to SUT B (A), demultiplexed or switched at SUT B (A), and transmitted to Tester B (A).

Test Procedure:

1. Insert traffic at SUTs A and B at rates at approximately 90% of the maximum rate that can be transported, and adjust the attenuators so that the system is operating error-free.
2. Adjust the frequency of Timing Reference A so that the bit rate of the STS-3c signal transmitted by SUT A is the worst-case rate that could occur if SUT A were free running (based on SUT A's internal clock accuracy specifications). Note if any bit errors or traffic interruptions occur.
3. If bit errors or traffic interruptions occur, adjust the Timing Reference frequencies to determine the combinations of offsets that cause errors.
4. If SUT A can be loop-timed and SUT B can be timed using a signal from an external source, then repeat the test set-up and procedure with the roles of SUT A and SUT B reversed.

Verdict Criteria:

The traffic should be error-free for all timing reference frequencies.

### 7. Test Case ID: STS3C/TC/3

| | |
|---|---|
| Test Case Name: | Performance under loop timing failure conditions. |
| Test Purpose: | This test is intended to verify that the signal transmitted by a loop-timed SUT can be received by the other SUT when the reference signal fails. |
| Pre-requisite: | One or both of the SUTs are capable of being loop-timed. |
| Reference: | [1], Section 2.1.1.2.1 |
| Test Configuration: | #6 |

Test Set-up:

1. Configure the system so that traffic originated by Tester A (B) is received by SUT A (B), multiplexed or switched to the STS-3c signal transmitted to SUT B (A), demultiplexed or switched at SUT B (A), and transmitted to Tester B (A).
2. Time SUT A using a reference signal from an external source, or allow it to free run. Loop time SUT B.

Test Procedure:

1. Insert traffic at SUTs A and B at rates at approximately 90% of the maximum data rate that can be transported, and adjust the attenuators so that the system is operating error-free.
2. Cause an LOS at SUT B's receiver.
3. Check the tester at SUT A for the received cell rate, and cell error rate. Also check the SONET Performance Monitoring registers at SUT A for B1, B2 and B3 coding violations.
4. If SUT A can be loop-timed, then repeat the test set-up and procedure with the roles of SUT A and SUT B reversed.

Verdict Criteria:

The traffic in one direction of transmission should still be error-free when there is an LOS in the other direction.

### 8. Test Case ID: STS3C/OH/1

| | |
|---|---|
| Test Case Name: | Interoperability for SONET section overhead generation and processing - I. |
| Test Purpose: | To verify BIP-8 conformance. |
| Pre-requisite: | Always run. |
| Reference: | [1], Sections 2.1.1.2.1 and 2.1.2.1.1 |
| Test Configuration: | #7 |

Test Set-up:

1. Establish a connection within SUT A.

Test Procedure:

1. Use the SUT B (SUT B can be replaced by test equipment) to introduce Section BIP-8 errors.
2. Check the Section Error Monitoring Function by monitoring the Section BIP-8 error counter (B1 coding violations counter) on SUT A.
3. Repeat the test procedure with the roles of SUT A and SUT B reversed.

Verdict Criteria:
In each case, the Section BIP-8 error counter on the receiving SUT should be incrementing.

**9. Test Case ID: STS3C/OH/2**

Test Case Name: Interoperability for SONET section overhead generation and processing - II.
Test Purpose: To verify Section BIP-8 interoperability.
Pre-requisite: Always run.
Reference: [1], Section 2.1.1.2.1
Test Configuration: #7

Test Set-up:
1. Connect the physical link between SUT A and SUT B.

Test Procedure:
1. Check the Section BIP-8 error counter (B1 coding violations counter) on each SUT.

Verdict Criteria:
Each SUT should be able to descramble the received data stream (generated at the other SUT) and process the Section overhead with no indication of Section BIP8 errors.

**10. Test Case ID: STS3C/OH/3**

Test Case Name: Interoperability for line layer overhead generation and processing - I.
Test Purpose: To verify BIP-24 conformance.
Pre-requisite: Always run.
Reference: [1], Sections 2.1.1.2.1 and 2.1.2.1.1
Test Configuration: #7

Test Set-up:
1. Establish a connection within SUT A.

Test Procedure:
1. Use the SUT B (SUT B can be replaced by test equipment) to introduce Line BIP-24 errors.
2. Check the Line Error Monitoring Function by monitoring the Line BIP-24 error counter (B2 coding violations counter) on SUT A.
3. Repeat the test procedure with SUT B in the role of SUT A.

Verdict Criteria:
In each case, the Line BIP-24 error counter on the receiving SUT should be incrementing.

**11. Test Case ID: STS3C/OH/4**

Test Case Name: Interoperability for line layer overhead generation and processing - II.
Test Purpose: To verify Line layer BIP-24 interoperability.
Pre-requisite: Always run.
Reference: [1], Section 2.1.1.2.1
Test Configuration: #7

Test Set-up:
1. Connect the physical link between SUT A and SUT B.

Test Procedure:

1. Check the Line BIP-24 error counter (B2 coding violations counter) on each SUT.

Verdict Criteria:
Each SUT should be able to process the Line overhead on the received data stream (generated at the other SUT) with no indication of Line BIP-24 errors.

### 12. Test Case ID: STS3C/OH/5

Test Case Name: Interoperability for line layer overhead generation and processing - III.
Test Purpose: To verify interoperability for the generation and processing of the Line FEBE.
Pre-requisite: Always run.
Reference: [1], Sections 2.1.1.2.1 and 2.1.2.1.1
Test Configuration: #8

Test Set-up:
1. Establish a connection through SUT A to SUT B.

Test Procedure:
1. Use the tester to generate traffic and introduce Line BIP-24 errors.
2. Check the Line Error Monitoring Functions by monitoring the Line BIP-24 error counter (B2 coding violations counter) on SUT A and the Line FEBE counter (Z2 counter) on SUT B.
3. Repeat the test procedure with the roles of SUT A and SUT B reversed.

Verdict Criteria:
In each case, the Line FEBE counter on one SUT should increment whenever a Line BIP-24 error count occurs on the other SUT.

### 13. Test Case ID: STS3C/OH/6

Test Case Name: Interoperability for path layer overhead generation and processing - I.
Test Purpose: To verify the proper generation and processing of the Path Error Monitoring Function on both SUTs.
Pre-requisite: Always run.
Reference: [1], Sections 2.1.1.2.1 and 2.1.2.1.1
Test Configuration: #7

Test Set-up:
1. Establish a connection within SUT A.

Test Procedure:
1. Use the SUT B (SUT B can be replaced by test equipment) to introduce Path BIP-8 errors.
2. Check the Path Error Monitoring Function by monitoring the Path BIP-8 error counter (B3 coding violations counter) on SUT A.
3. Repeat the test procedure with SUT B in the role of SUT A.

Verdict Criteria:
In each case, the Path BIP-8 error counter on the receiving SUT should be incrementing.

### 14. Test Case ID: STS3C/OH/7

Test Case Name: Interoperability for path layer overhead generation and processing - II.
Test Purpose: To verify interoperability for Path BIP-8 generation and processing.
Pre-requisite: Always run.
Reference: [1], Section 2.1.1.2.1
Test Configuration: #7

Test Set-up:
1. Connect the physical link between SUT A and SUT B.

Test Procedure:

1. Check the Path BIP-8 error counter (B3 coding violations counter) on each SUT.

Verdict Criteria:

Each SUT should be able to process the Path overhead on the received data stream (generated at the other SUT) with no indication of Path BIP-8 errors.

### 15. Test Case ID: STS3C/OH/8

Test Case Name: Interoperability for path layer overhead generation and processing - III.
Test Purpose: To verify interoperability for the generation and processing of the Path FEBE.
Pre-requisite: Always run.
Reference: [1], Sections 2.1.1.2.1 and 2.1.2.1.1
Test Configuration: #8

Test Set-up:

1. Establish a connection through SUT A to SUT B.

Test Procedure:

1. Use the tester to generate traffic and introduce Path BIP-8 errors.
2. Check the Path Error Monitoring Functions by monitoring the Path BIP-8 error counter (B3 coding violations counter) on SUT A and the Path FEBE counter (G1 counter) on SUT B.
3. Repeat the test procedure with the roles of SUT A and SUT B reversed.

Verdict Criteria:

In each case, the Path FEBE counter on one SUT should increment whenever a Path BIP-8 error count occurs on the other SUT.

### 16. Test Case ID: STS3C/PS/1

Test Case Name: Interoperability for B-ISDN specific TC sublayer functions - I.
Test Purpose: To verify interoperability for cell scrambling and descrambling.
Pre-requisite: Always run.
Reference: [1], Section 2.1.1.2.2.2
Test Configuration: #4

Test Set-up:

1. Establish a bidirectional connection between SUT A and SUT B.

Test Procedure:

1. Using the ATM testers, send SONET STS-3c payload from SUT A to SUT B and from SUT B to SUT A.

Verdict Criteria:

Traffic should be passed by both SUTs without cell loss or corruption. No detection of errors or indication of alarms related to cell scrambling and descrambling should be noticed.

### 17. Test Case ID: STS3C/CDL/1

Test Case Name: Interoperability for B-ISDN specific TC sublayer functions - II.
Test Purpose: To verify interoperability for cell mapping and cell delineation.
Pre-requisite: Always run.
Reference: [1], Sections 2.1.1.2.2.3 and 2.1.1.2.2.4
Test Configuration: #4

Test Set-up:

1. Establish a bidirectional connection between SUT A and SUT B.

Test Procedure:

1. Using the ATM testers, send SONET STS-3c payload from SUT A to SUT B and from SUT B to SUT A.

Verdict Criteria:

Traffic should be passed by both SUTs without cell loss or corruption. No detection of errors or indication of alarms related to cell mapping and cell delineation should be noticed.

### 18. Test Case ID: STS3C/HEC/1

| | |
|---|---|
| Test Case Name: | HEC interoperability test. |
| Test Purpose: | To verify interoperability in HEC calculations. |
| Pre-requisite: | Always run. |
| Reference: | [1], Section 2.1.1.2.2.1 |
| Test Configuration: | #4 |

Test Set-up:

1. Establish appropriate connections on both SUTs to pass uni-directional traffic from SUT A to SUT B.
2. Configure the Tester A to generate cells at 90% of the date rate with GFI field set to 0.

Test Procedure:

1. Use the Tester A to generate cells from SUT A to SUT B.
2. Verify that no cells are dropped in both directions.
3. Verify also that SUT B does not raise any HEC errors on the cells generated by SUT A.
4. Repeat this test with the relative positions of SUTs A and B interchanged.

Verdict Criteria:

The calculation of HEC is interoperable if no cells are dropped and no HEC errors are encountered by both SUTs.

# 6. 100 Mbps Multimode Fibre Physical Layer Test Suite

## 6.1 Test Case Index

| No. | Test Case ID | Test Case Name | UNI 3.0 Reference | Test Config. # |
|---|---|---|---|---|
| 1 | 100Mbps/LOS/1 | Recovery from loss of signal | None | 1 |
| 2 | 100Mbps/PMD/1 | Optical signal | None | 7 |
| 3 | 100Mbps/PMD/2 | 4B/5B line coding | 2.3.1.2 | 7 |
| 4 | 100Mbps/CDL/1 | Cell delineation | 2.3.2.2 | 1 |
| 5 | 100Mbps/HEC/1 | HEC interoperability test | 2.3.2.3 | 4 |

## 6.2 Test Cases Dynamic Behavior

**1. Test Case ID: 100Mbps/LOS/1**

Test Case Name: Recovery from loss of signal.
Test Purpose: To verify the recovery of signal levels, line coding, line rates, and bit timing.
Pre-requisite: Unconditional.
Reference: None
Test Configuration: #1

Test Set-up:

1. Connect the physical link between the two SUTs.
2. Establish appropriate circuit connections within SUTs A and B to pass traffic from SUT A to SUT B and vice versa.
3. Use the two testers to cause traffic to flow from SUT A to SUT B and vice versa at 90% of the maximum data rate.

Test Procedure:

1. Break the physical link connecting the two SUTs.
2. Ensure that both SUTs acknowledge that signal is lost and ATM traffic stops to flow.
3. Reconnect the two SUTs.
4. Observe that the optical signal is restored and ATM traffic begins to flow again.

Verdict Criteria:

Optical signal should be restored automatically and no cells should be dropped or corrupted after the physical link is re-established. In addition, all alarms that have been raised when the link was broken should be cleared.

**2. Test Case ID: 100Mbps/PMD/1**

Test Case Name: Optical signal.
Test Purpose: To verify interoperability in the optical signal.
Pre-requisite: Conditional on the availability of 4B/5B line coding error counts.
Reference: None
Test Configuration: #7

Test Set-up:
1. Connect the physical link between the two SUTs.

Test Procedure:
1. Observe that each SUT indicate that it is able to detect the optical signal sent by the other SUT.

Verdict Criteria:
Each SUT should indicate that it is able to detect the optical signal transmitted by the other SUT.

**3. Test Case ID: 100Mbps/PMD/2**

Test Case Name: 4B/5B line coding.
Test Purpose: To verify interoperability in the 4B/5B line coding.
Pre-requisite: Unconditional.
Reference: [1], Section 2.3.1.2
Test Configuration: #7

Test Set-up:
1. Connect the physical link between the two SUTs.

Test Procedure:
1. Observe that the code violations error counter is not increasing.

Verdict Criteria:
The code violations error counter of both SUTs should not increase.

**4. Test Case ID: 100Mbps/CDL/1**

Test Case Name: Cell delineation.
Test Purpose: To verify interoperability in cell delineation.
Pre-requisite: Unconditional.
Reference: [1], Section 2.3.2.2
Test Configuration: #1

Test Set-up:
1. Connect the physical link between the two SUTs.
2. Establish appropriate virtual circuit connections.
3. Use the Tester A to generate ATM traffic at 90% of the full data rate.

Test Procedure:
1. Observe that no cells are dropped or corrupted.
2. Repeat this test with the relative positions of SUTs A and B reversed.

Verdict Criteria:
Both SUTs should be able to acquire cell delineation and no cells lost or corrupted.

**5. Test Case ID: 100Mbps/HEC/1**

Test Case Name: HEC interoperability test.
Test Purpose: To verify interoperability in HEC calculations.
Pre-requisite: Always run.
Reference: [1], Section 2.3.2.3
Test Configuration: #4

Test Set-up:

1. Establish appropriate connections on both SUTs to pass uni-directional traffic from SUT A to SUT B.
2. Configure the Tester A to generate cells at 90% of the date rate with GFI field set to 0.

Test Procedure:

1. Use the Tester A to generate cells from SUT A to SUT B.
2. Verify that no cells are dropped in both directions.
3. Verify also that SUT B does not raise any HEC errors on the cells generated by SUT A.
4. Repeat this test with the relative positions of SUTs A and B interchanged.

Verdict Criteria:

The calculation of HEC is interoperable if no cells are dropped and no HEC errors are encountered by both SUTs.