UP2000
Technical Reference Manual

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Alpha Processor, Inc.
A Samsung Company
130C Baker Avenue Extension
Concord, MA 01742
Tel: 978.318.1100
Fax: 978.371.3177

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Revision History

Date	Rev	Description
07/06/99	**51-0029-0A**	**UP2000 Technical Reference Manual initial release.**
07/13/99	51-0029-0Arev2	UP2000 Technical Reference Manual second review.
07/21/99	**51-0029-0Arev3**	**UP2000 Technical Reference Manual third review.** **This publication describes the UP2000 Motherboard part number 40-0005-F.** **Future versions of the TRM will have change bars turned on to track changes to the information presented.**
07/29/99	51-0029-1A	UP2000 Technical Reference Manual first product release. Alpha Slot B Cartridge renamed Alpha Slot B Module.
10/21/99	**51-0029-2A**	**API Acceptance of UP2000 Technical Reference Manual.**
4/07/00	51-0029-3A	Modified the following information: • Firmware platform moved to Reset PAL code, Alpha SRM Console and Alpha Diagnostics • COM1 port reserved for serial console devices • Add remote reset capabilities • Add thermal sensitivity information

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Preface

Overview

This manual describes the Alpha Processor, Inc. (API) UP2000 product, including the UP2000 Motherboard used with the Alpha Slot B Module, for computing systems based on Samsung's Alpha 21264 microprocessor and the Compaq 21272 core logic chipset.

Audience

This manual is intended for system designers and others who use the UP2000 to design or evaluate computer systems based on the Alpha Slot B Module with the 21264 microprocessor and the 21272 core logic chipset.

Scope

This manual describes the features, configuration, functional operation, and interfaces of the UP2000. This manual does not include specific details on industry standards (for example, on PCI or ISA bus specifications). Additional information is available in the appropriate vendor and IEEE specifications. See Appendix B for information on how to order related documentation and obtain additional technical support.

Manual Organization

The UP2000 Technical Reference Manual is organized as follows:

- Chapter 1, "UP2000 Introduction," contains a description of the UP2000's features. A functional block diagram of the UP2000 is included.
- Chapter 2, "System Configuration," describes the UP2000 configuration options, including jumper functions and settings. Board layouts are provided, which identify component locations.
- In Chapter 3, "Electrical, Environmental and Physical Data," a description is provided of the electrical and environmental requirements and physical board dimensions for the UP2000.
- A functional description of the UP2000 is provided in Chapter 4, "Functional Description." This includes the 21272 core logic chipset and a brief description of its implementation with the 21264 microprocessors.

Descriptions of the functional subsystems, logic design and firmware design for the UP2000 are also provided.

- Chapter 5, “System Memory and Address Mapping,” provides a description of the memory subsystem and address mapping for the UP2000.
- Pinouts for the Alpha Slot B Connector and all power connectors used in the UP2000 are provided in Appendix A, “Connectors and Pinouts.” This appendix also contains a list of all other connectors used in the UP2000, which are industry standard parts.
- Appendix B, “Support, Products and Documentation,” describes how to obtain technical information and support for the UP2000, and where to order parts and accessories for the UP2000. It includes information on how to obtain API products and supporting literature.

Conventions and Definitions

This section defines product-specific terminology, abbreviations, and other conventions used throughout this manual.

Signals and Bits

- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by API for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes to these registers, it must first read the register and change only the non-reserved bits before writing back to the register.

Data

The following list defines data terminology:

- Units
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.

- Abbreviations—The following notation is used for bits and bytes:
  - Kilo—K, as in 4-Kbyte page (2^{10})
  - Mega—M, as in 4 Mbits / sec (2^{20})
  - Giga—G, as in 4 Gbytes of memory space (2^{30})

Acronyms

The following is a list of the acronyms used in this document and their definitions.

Abbreviation	Meaning
API	**Alpha Processor, Inc.**
BIOS	Basic Input / Output System
BIST	**Built-In Self Test**
CE	European Conforming
CSR	**Control/Status Register**
CPU	Central Processing Unit
CUL	**Canadian Underwriters Laboratory**
DBM	Debug Monitor
DIMM	**Dual Inline Memory Module**
DMA	Direct Memory Access
DRAM	**Direct Random Access Memory**
DQM	Data Input / Output Mask
EIDE	**Enhanced Integrated Device Electronics**
EMI	Electromagnetic Interference
EPLD	**Electrically Programmable Logic Device**
ESBGA	Enhanced Super Ball Grid Array
FCC	**Federal Communications Commission**
FDC	Floppy Disk Controller
FDD	**Floppy Disk Drive**
FID	Frequency Identification
FIFO	**First In, First Out**
FPGA	Field Programmable Gate Array
HDD	**Hard Disk Drive**
I^2C	Inter-integrated Circuit
IDE	**Integrated Device Electronics**

Abbreviation	Meaning
I/O	Input/Output
ISA	**Industry Standard Architecture**
ISP	In-system Programmability
LED	**Light Emitting Diode**
LVD	Low Voltage Differential
LVTTL	**Low Voltage Transistor-Transistor Logic**
NDA	Non-disclosure Agreement
OEM	**Original Equipment Manufacturer**
OS	Operating System
PAL	**Privileged Architecture Library**
PCB	Printed Circuit Board
PCI	**Peripheral Component Interconnect**
PIO	Programmed Input/Output
PLL	**Phase Locked Loop**
ROM	Read-only Memory
RTC	**Real-time Clock**
SCSI	Small Computer System Interface
SDRAM	**Synchronous Direct Random Access Memory**
SE	Single-ended
SPD	**Serial Presence Detect**
SROM	Serial Read-only Memory
SRAM	**Static Random Access Memory**
SRM	System Reference Manual
SSRAM	**Synchronous SRAM**
TIG	TTL Integrated Glue Logic
UL	**Underwriters Laboratory**
USB	Universal Serial Bus
VRM	**Voltage Regulator Module**

Chapter 1 UP2000 Introduction

This chapter provides an overview of the UP2000 product, including its components and features.

The UP2000 product consists of a UP2000 Motherboard and one or two Alpha Slot B Modules. The Alpha Slot B Module consists of the 21264 microprocessor, Bcache (level 2 cache) and voltage converters to convert from 12 or 5 volts to between 2.2 and 1.5V.

Note: *The position in which you use an Alpha Slot B Module on the UP2000 Motherboard, primary connection or secondary connection, determines the following:*

- *J23 provides the connection for the primary, or first, Alpha Slot B Module and runs on 12V*
- *J22 provides the connection for the secondary, or second, Alpha Slot B Module and runs on 5V*

1.1 Features

Table 1-1 provides a summary of the UP2000 product features.

Table 1-1 UP2000 Product Features

Feature	Description	Manufacturer
Physical Form Factor:	**ATX Extended (12 inch X 13 inch)**	
Daughter Card Interface:	Supports one or two Alpha Slot B Modules using the Alpha 21264 microprocessor, at speeds of 667 or 750 MHz	Alpha Processor, Inc.
Chipset:	**21272 (Tsunami)—One Cchip, four Dchips, and two Pchips provide the following:**	**Compaq**
	• Maximum 83 MHz system bus with Double Data Rate (DDR) transfers, maximum bandwidth of 2.67 GBytes / second	
	• **One 256-bit memory bus**	
	• One 64-bit, 33 MHz PCI bus with two 64-bit slots and one 32-bit slot, and one 32-bit, 33 MHz PCI bus with three 32-bit slots	

Table 1-1 UP2000 Product Features (Continued)

Feature	Description	Manufacturer
Cache:	**External Bcache with 128-bit data path for an Alpha Slot B Module supports:**	
	• 2 MB or 4 MB cache per 667 MHz processor	
	• **4 MB or 8 MB cache per 750 MHz processor**	
	• Late Write (LW) Synchronous SRAMS (SSRAMs)	
Main Memory:	• **Eight 168-pin Dual Inline Memory Module (DIMM) sockets, up to 2 GB (256 MB per DIMM)**	
	• Supports Phase Locked Loop (PLL) or Register-based Synchronous Direct Random Access Memory (SDRAM) Serial Presence Detect (SPD) modules of 64 MB, 128 MB, and 256 MB	
	• **Low Voltage Transistor-Transistor Logic (LVTTL) compatible memory I/O**	
Power:	ATX power connector, supplying +3.3 Vdc, ± 5 Vdc, and ± 12 Vdc	
On-board I/O:	• **CY82C693UB Peripheral Component Interconnect (PCI)/Industry Standard Architecture (ISA) Bridge (PCI Local Bus Specification Revision 2.1 compliant), Enhanced Integrated Device Electronics (EIDE) controller, and two Universal Serial Bus (USB) ports**	**Cypress**
	• AIC-7891 Small Computer System Interface (SCSI) Controller (Ultra2 SCSI), connections for up to 15 SCSI devices	Adaptec
	• **FDC37C669 Super Input/Output (I/O) Controller—2.88 MB Floppy Disk Controller (FDC), Parallel port, two NS16C550-compliant Serial ports, Real-time Clock (RTC) port, Keyboard, and Mouse**	**SMC**
I/O Slots:	• Four 32-bit, 33 MHz PCI Slots, PCI Local Bus Specification Revision 2.1 compliant	
	• **Two 64-bit, 33 MHz PCI Slots, PCI Local Bus Specification Revision 2.1 compliant**	
	• One ISA Slot (Shared)	
Firmware:	**Embedded Alpha System Reference Manual (SRM) Console**	
System Management (via PCI-ISA Bridge I^2C Controller PCF8584):	• Monitoring of processor thermal state	**Philips**
	• **Detection of processor asset record**	

1.2 System Components

The UP2000 is implemented in industry-standard parts and uses one or two 21264 central processing units (CPUs). The functional components of the UP2000 are shown in block diagram form in Figure 1-1. A detailed description of system components is provided in Chapter 4, "Functional Description".

Note: *Refer to the list of Acronyms on page xii of the Preface for an explanation of terminology used in the block diagram.*

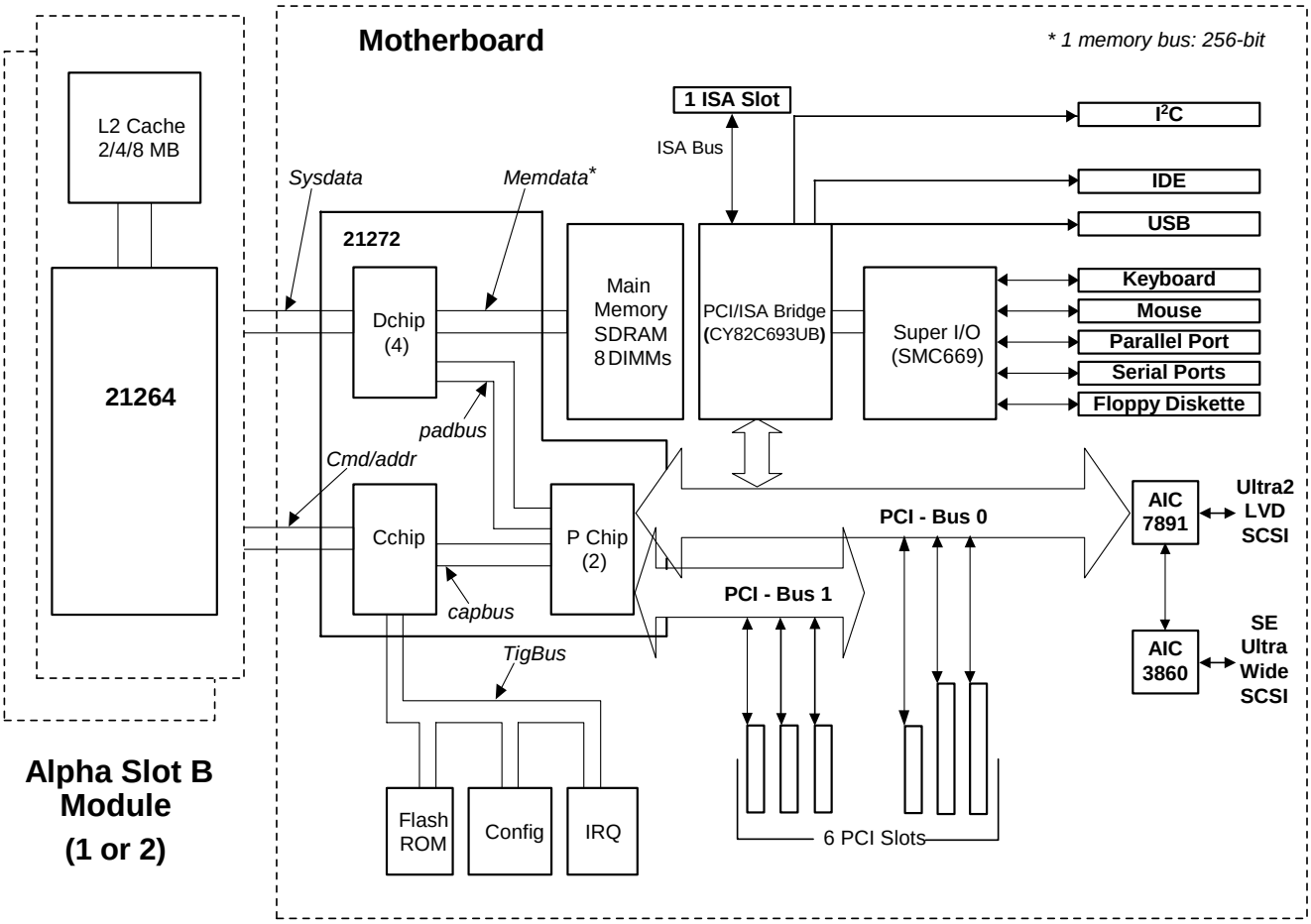


Figure 1-1 UP2000 Functional Block Diagram

Chapter 2 System Configuration

This chapter describes the layout and configuration of the UP2000 Motherboard and the Alpha Slot B Module.

2.1 Board Layouts and Components

The UP2000 uses jumpers to implement variations in clock frequency for the 21272 and 21264, and for Bcache configuration. Jumpers for the 21264 speed and Bcache configuration are located on the UP2000 Motherboard. You must configure these jumpers according to the configuration of the Alpha Slot B Module.

On-board connectors are provided for the following:

- I/O
- Memory DIMMs
- Serial and parallel peripherals
- SCSI devices
- Integrated device electronics (IDE) devices

These connectors and the configuration jumpers are shown in Figure 2-1, which depicts the UP2000 Motherboard and its components. Table 2-1 specifies the components as indicated in Figure 2-1.

Refer to Appendix A for a complete description of the connectors and pinouts used in the UP2000.

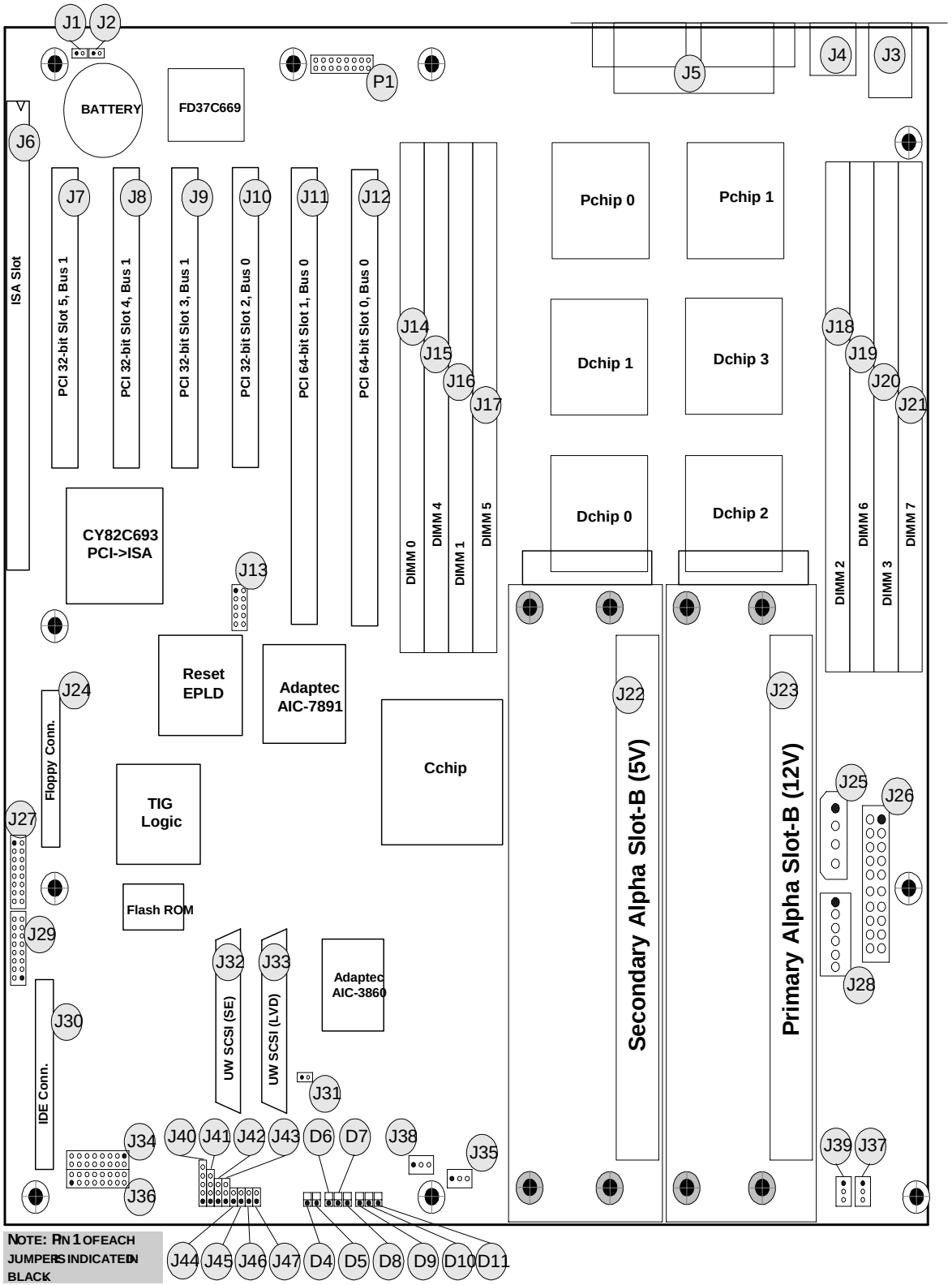


Figure 2-1 UP2000 Motherboard Layout

Table 2-1 UP2000 Motherboard Jumper and Connector Component List

Comp. No.	Specification	Comp. No.	Specification
J1	**System Chassis Fan Connector**	**J2**	**System Chassis Fan Connector**
J3	Keyboard / Mouse Connector	J4	USB Connector
J5	**D-SUB Connector (Serial IO/ Parallel IO)***	**J6**	**ISA Expansion Bus Connector**
J7	32-bit PCI Slot 5, Bus 1 Connector	J8	32-bit PCI Slot 4, Bus 1 Connector
J9	**32-bit PCI Slot 3, Bus 1 Connector**	**J10**	**32-bit PCI Slot 2, Bus 0 Connector**
J11	64-bit PCI Slot 1, Bus 0 Connector	J12	64-bit PCI Slot 0, Bus 0 Connector
J13	**Reset Electrically Programmable Logic Device (EPLD) In-system Programmability (ISP) Connector**	**J14**	**168-pin DIMM 0 Socket**
J15	168-pin DIMM 4 Socket	J16	168-pin DIMM 1 Socket
J17	**168-pin DIMM 5 Socket**	**J18**	**168-pin DIMM 2 Socket**
J19	168-pin DIMM 6 Socket	J20	168-pin DIMM 3 Socket
J21	**168-pin DIMM 7 Socket**	**J22**	**Alpha Slot B Connector for Secondary Module (5V)**
J23	Alpha Slot B Connector for Primary Module (12V)	J24	Floppy Drive Connector
J25	**Alpha Slot B Module Power Connector (4 pin)**	**J26**	**ATX Power Connector (20 pin)**
J27	System Configuration Jumper	J28	AUX ATX (Optional) Power Connector for 3.3V (6 pin)
J29	**Configuration Jumper**	**J30**	**IDE Bus Connector**
J31	Not Used	J32	Ultra-wide SCSI Single-ended (SE) Connector
J33	**Ultra-wide SCSI Low Voltage Differential (LVD) Connector**	**J34**	**CPU Speed/Flash_Sel Jumper**
J35	Alpha Slot B Module Fan Connector (Secondary)	J36	Bcache Configuration Jumper
J37	**Alpha Slot B Module Fan Connector (Primary)**	**J38**	**Alpha Slot B Module Fan Connector (Secondary)**
J39	Alpha Slot B Module Fan Connector (Primary)	J40	Power Light Emitting Diode (LED) Connector
J41	**Speaker Connector**	**J42**	**Secondary Alpha Slot B Module Debug Port Connector**

Note: ***Connector J5 includes the COM1 and COM2 ports. COM1 is reserved for a serial console device. Connect all other serial devices to COM2 or any expansion serial ports.***

Table 2-1 UP2000 Motherboard Jumper and Connector Component List (Continued)

Comp. No.	Specification	Comp. No.	Specification
J43	Primary Alpha Slot B Module Debug Port Connector	J44	Power Button Connector
J45	**Halt Button Connector**	**J46**	**SCSI LED Connector**
J47	Reset Button Connector		

Note: ***Connector J5 includes the COM1 and COM2 ports. COM1 is reserved for a serial console device. Connect all other serial devices to COM2 or any expansion serial ports.***

2.2 Configuration Jumpers

The UP2000 Motherboard has four programmable jumper blocks, located at J27, J29, J34, and J36. Locations of J27, J29, J34 and J36 are shown in Figure 2-2, on the front left side of the UP2000 Motherboard. Table A-5 in section A.3, ”Configuration Jumper Pinouts,” on page A-8 provides a complete list of the pinouts for these jumpers.

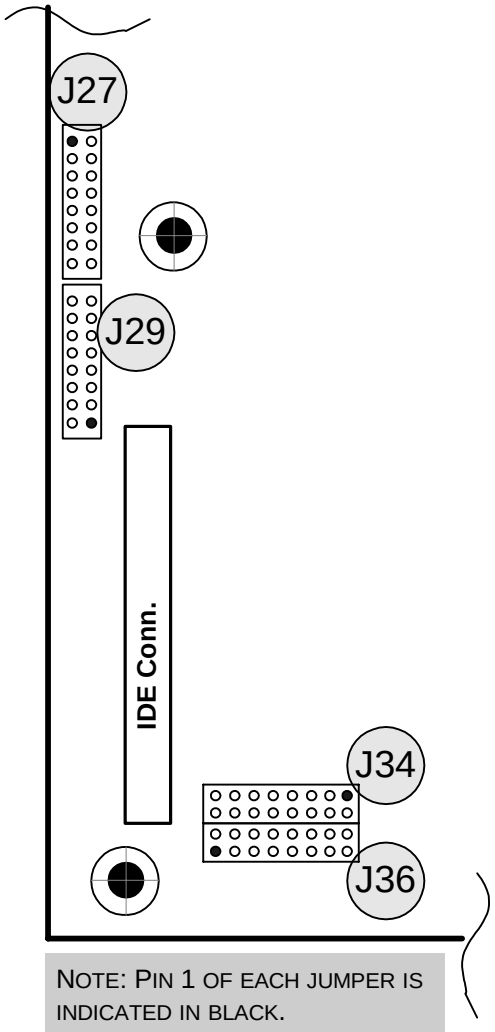


Figure 2-2 Configuration Jumpers

The configuration jumpers each define 8 bits of data. Configuration bits for the UP2000 are defined in Table 2-2.

Table 2-2 Configuration Bits

Bit	Configuration Jumper			
	J27	J29	J34	J36
Bit 0 (pins 0 and 1)	**TIG Data 7**	**Alpha Diagnostics**	**Flash Select 2**	**Primary Bcache Configuration 0**
Bit 1 (pins 2 and 3)	TIG Data 6	Memory Timing, Primary CPU	Flash Select 1	Primary Bcache Configuration 1
Bit 2 (pins 4 and 5)	**TIG Data 5**	**Memory Timing, Secondary CPU**	**Flash Select 0**	**Primary Bcache Configuration 2**
Bit 3 (pins 6 and 7)	TIG Data 4	Reset PAL code Mini-Debug	Flash Select Bypass	Primary Bcache Configuration 3
Bit 4 (pins 8 and 9)	**TIG Data 3**	**21272 Speed 0**	**CPU Speed 0**	**Secondary Bcache Configuration 0**
Bit 5 (pins 10 and 11)	TIG Data 2	21272 Speed 1	CPU Speed 1	Secondary Bcache Configuration 1
Bit 6 (pins 12 and 13)	**Spare**	**21272 Speed 2**	**CPU Speed 2**	**Secondary Bcache Configuration 2**
Bit 7 (pins 14 and 15)	Flash Write Protection	Password Bypass	Spare	Secondary Bcache Configuration 3

UP2000 configuration bit settings for jumpers J27, J29, and J34 are shown in Figure 2-3. Settings for J27, J29, and J34 vary depending on CPU speed selected.

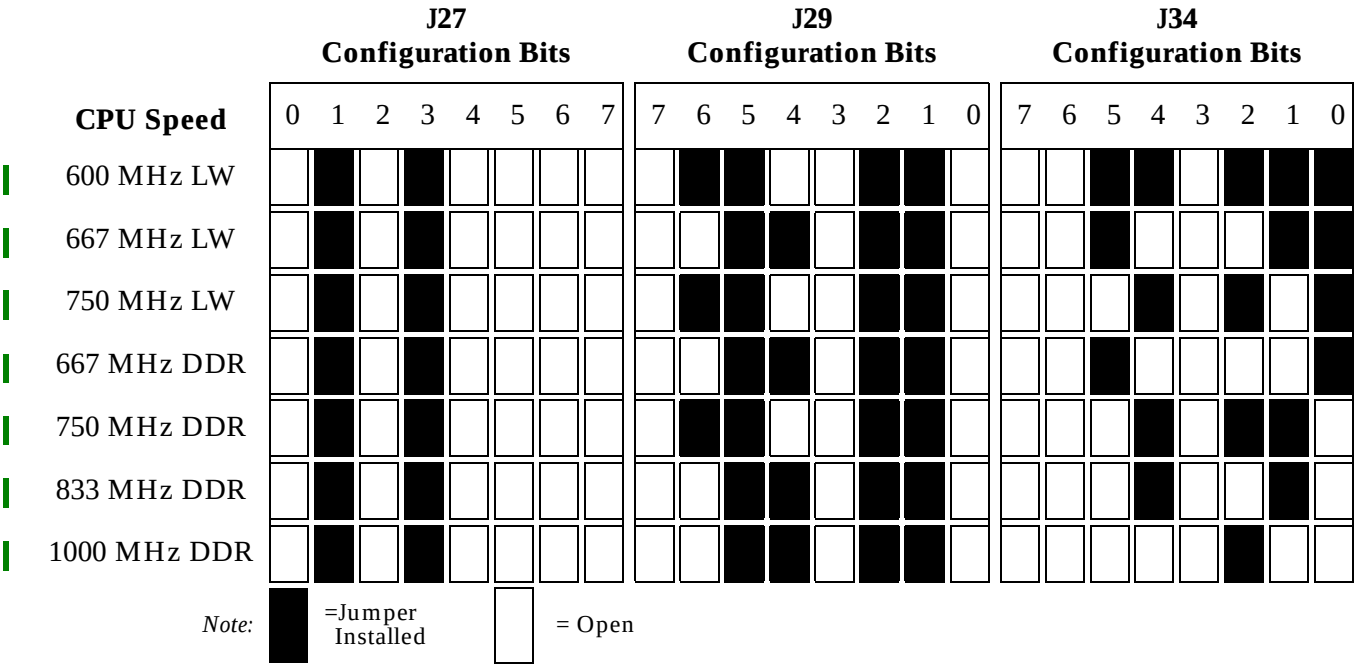


Figure 2-3 Configuration Settings for J27, J29, and J34

UP2000 configuration bit settings for J36 are shown in Figure 2-4. These settings vary depending on Bcache size selected.

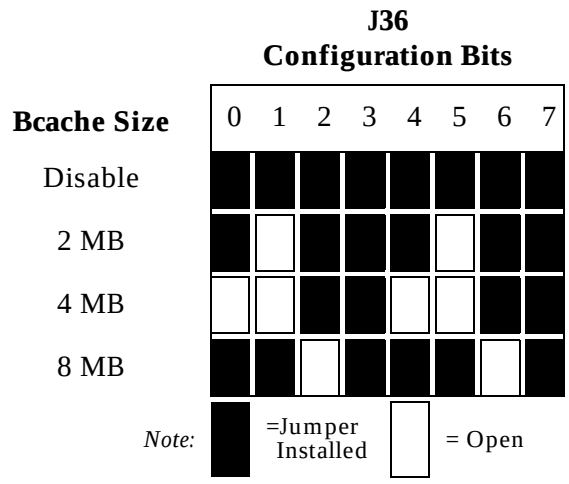


Figure 2-4 Configuration Settings for J36

2.2.1 Diagnostics and Flash Recovery

The Alpha Diagnostics utility provides the emergency recovery mechanism when the primary firmware image contained in flash memory is corrupted. When flash memory is corrupted, and no image can be loaded safely from the flash ROM, you can run Alpha Diagnostics and boot another image from a diskette that is capable of reprogramming the flash ROM.

By default, a jumper is not installed on pins 0 and 1 (bit 0) of J29 on the UP2000 Motherboard (the OFF position), and Alpha Diagnostics is not enabled.

Configuration of diagnostics and flash recovery is managed through settings of pins 0–1, 6–7, and 14–15 of J29. Table 2-3 shows the possible configuration settings for diagnostics and flash recovery of the UP2000. The default function is Normal Boot Sequence, with no shunts installed on pins 0–1, 6–7, and 14–15 of J29.

Note: *All remaining jumpers on J29 must remain in the default positions. These jumpers control other functions.*

Table 2-3 Diagnostics and Flash Recovery Configuration Settings (J29)

Function	Install Jumper on Pins:		
	0/1	6/7	14/15
Normal Boot Sequence (using firmware)—Default	**0**	**0**	**0**
Restore Factory Defaults (Bypass password check)	0	0	1
Normal Recovery (using firmware)	**1**	**0**	**0**
Alpha Diagnostics Recovery (using firmware)	1	0	1

Notes: ***1. 0 = No shunt installed. 1 = Shunt installed.***

2. The Debug Ports (primary Alpha Slot B Module port J43 and secondary Alpha Slot B Module port J42) default to 9600 baud. When using the Interactive Reset PAL code function, type an uppercase U to set the interactive baud rate higher.

3. Refer to section 4.4.2 on page 4-24 for information on Reset PAL code.

4. Refer to section 4.4.3 on page 4-24 for information on Alpha Diagnostics.

Table 2-3 Diagnostics and Flash Recovery Configuration Settings (J29) (Continued)

Function	Install Jumper on Pins: 0/1	6/7	14/15
Interactive Alpha Diagnostics (using operator console)	**1**	**1**	**0**
Interactive Alpha Diagnostics (using Debug Port J42/J43)	1	1	1
Interactive Reset PAL Code (using Debug Port J42/J43)	**0**	**1**	**0**

Notes: ***1. 0 = No shunt installed. 1 = Shunt installed.***

2. The Debug Ports (primary Alpha Slot B Module port J43 and secondary Alpha Slot B Module port J42) default to 9600 baud. When using the Interactive Reset PAL code function, type an uppercase U to set the interactive baud rate higher.

3. Refer to section 4.4.2 on page 4-24 for information on Reset PAL code.

4. Refer to section 4.4.3 on page 4-24 for information on Alpha Diagnostics.

2.2.2 Memory Timing

Memory bus timing is controlled by jumper settings on pins 2 through 5 (bits 1 and 2) of J29. Both jumpers are OFF by default, and they must remain OFF.

2.2.3 Mini-Debugger

The Alpha Reset PAL code mini-debugger is enabled / disabled by pins 6 and 7 (bit 3) of J29 on the UP2000 Motherboard (see Figure 2-1). The default position for this jumper is OFF. When this jumper is ON, the Reset PAL code initialization traps to the mini-debugger after all initialization is completed, but before starting the execution of the system flash ROM code.

2.2.4 Password Bypass

If the use of passwords is enabled and you forget the current password, there are ways to bypass password protection under the Alpha System Reference Manual (SRM) console.

The Alpha SRM console requires a password only after the Set Secure command has been issued. To clear a password if you forget the value:

1. Enter the Login command.
2. At the Enter Password prompt:
   a. Press the Halt button.
   b. Press Enter.

The password is now cleared and the console cannot be put into secure mode until a new password is set.

2.2.5 Flash Write Protection

The UP2000 provides write protection for the firmware flash ROM. By default, a jumper is installed on pins 14 and 15 (bit 7) of J27 on the UP2000 Motherboard (the OFF position), and writing to the flash ROM is not enabled.

2.2.6 System Speed

The system base frequency system is determined by pins 8–9, 10–11 and 12–13 (bits 4, 5 and 6) of J29 on the UP2000 Motherboard. The valid configurations for these jumpers are as follows:

- 83 MHz: Pins 8–9 and 10–11 are jumpered, Pins 12–13 are open
- 75 MHz: Pins 8–9 are open, Pins 10–11 and 12–13 are jumpered

Alpha Slot B Module processors that run at 600 and 750 MHz require a base system speed of 75 MHz. Alpha Slot B Module processors that run at 667, 833, and 1000 MHz require a base system speed of 83 MHz.

Chapter 3 Electrical, Environmental and Physical Data

In this chapter, a description is provided of the UP2000 power requirements, environmental and enclosure specifications, and physical parameters.

3.1 Power Specifications

3.1.1 Power Connectors

The power connectors specified to support dual Alpha Slot B Modules are as follows:

- ATX Standard: One 10 x 2 (20-pin)
- AUX ATX: One 6 x 1 (6-pin)
- Alpha Slot B Module Power Supply: One 4 x 1 (4-pin)

12V is input to the L7571C Voltage Regulator Module (VRM), which outputs the core voltage to the CPU. Because over 9A is required by the Alpha Slot B Module, one Alpha Slot B Module Power Supply 4 x 1 (4-pin) connector is added. To support 3.3V, an AUX ATX 6 x 1 (6-pin) connector is used.

3.1.2 Estimated Power Consumption

The UP2000 Motherboard has a maximum total power consumption of 97.05W. The primary Alpha Slot B Module has a maximum total power consumption of 165.8W, while the secondary Alpha Slot B Module has a maximum total power consumption of 142W.

Table 3-1 lists the current requirement for each direct current supply voltage (Vdc) for the UP2000 Motherboard. Table 3-2 and Table 3-3 list the current requirement for each direct current supply voltage (Vdc) for the primary and secondary Alpha Slot B Modules, respectively. All requirements assume maximum usage applied.

Note: *These tables do not include requirements for SDRAM, peripheral slots or disk drives. Be sure to allow for adequate additional current when selecting a power supply for the UP2000.*

Table 3-1 Estimated Power Consumption–UP2000 Motherboard

V_{DD} Source	Current	Power	Remarks
3.3V	**17.2A**	**56.8W**	
5V	6.8A	34.0W	
-5V	**0.05A**	**0.25W**	
12V	0.4A	4.8W	Fans
-12V	**0.1A**	**1.2W**	
Total Power Consumption:		**97.05W**	

Table 3-2 Estimated Power Consumption–Primary Alpha Slot B Module, 8 MB Bcache

V_{DD} Source	Current	Power	Remarks
3.3V	**6.3A**	**20.8W**	
5V	0.2A	1.0W	
12V	**12A**	**144W**	**VRM**
Total Power Consumption:		**165.8W**	

Table 3-3 Estimated Power Consumption–Secondary Alpha Slot B Module, 8 MB Bcache

V_{DD} Source	Current	Power	Remarks
3.3V	**6.3A**	**20.8W**	
5V	24A	120W	VRM
12V	**0.1A**	**1.2W**	
Total Power Consumption:		**142.0W**	

3.1.3 Power Supply

The UP2000 requires the use of a 600W ATX power supply. Refer to Application Note 51-0038-0A, *MACASE Chassis RFI Upgrade Kit*, for

specific information about the power supply requirements.

3.2 Environmental Specifications

Each 21264 microprocessor is cooled by two small fans blowing directly into the chip's heat sink. The UP2000 is designed to run efficiently using only these fans. Additional fans may be necessary depending upon cabinetry and requirements of plug-in cards.

The UP2000 Motherboard and Alpha Slot B Module are specified to run within the environment listed in Table 3-4.

Table 3-4 Environmental Requirements

Parameter	Specification
Operating temperature	**+5 to +35° C (+41 to +95° F)**
Storage temperature	-35 to +85° C (-31 to +185° F)
Relative Humidity	**10% to 90%, with maximum wet bulb temperature of 35° C (95° F) and minimum dew point of 2° C (36° F)**
Rate of (dry bulb) temperature change	11° C / hr. ±2° C / hr. (20° F / hr. ±4° F / hr.)

3.2.1 Safety

The UP2000 Motherboard meets registered product-safety certification for the U.S. and Canadian Underwriters Laboratories (UL and CUL). It also meets the European Conforming (CE) standard EN60950:1992 "Safety of Information Technology Equipment Including Electrical Business Equipment Incorporating Amendment Nos 1, 2, 3, 4." European Norm (EN) standards which conform to the relevant directives are published in the Official Journal of the European Community.

3.2.2 EMI

Note: *API recommends the use of high-quality, shielded cables for all I/O.*

The UP2000 meets electro-magnetic interference (EMI) emission certification for the following:

- Federal Communications Commission (FCC) 47 CFR Part 15 Class A (USA)
- EN 55022:1994 / A1:1995 / A2:1997 Class A ITE emissions requirements (EU)
- ICES-003 Issue 3 Class A Digital Apparatus (Canada)
- VCCI Class A ITE (Japan)
- AS / NZS 3548:1995 / CISPR 22 Class A ITE (Australia)
- SABS CISPR 22:1993 Class A ITE (South Africa)

Note: *Application Note 51-0038-0A contains detailed information about requirements for EMI certification notices which must appear on assemblies that use the UP2000.*

The UP2000 also meets the EMI immunity certification EN 50082-1:1992 "EMC Residential, Commercial and Light Industrial Generic Immunity Standard."

3.2.3 Thermal

Figure 3-1 shows the location of thermally-sensitive components on the UP2000 Motherboard. A list of maximum allowable case temperatures for these components is provided in Table 3-5.

Case temperatures are a vital factor in determining airflow on a motherboard. Variables which may affect a component's case temperature include the following:

- Operating temperature
- Operating frequency
- Current load

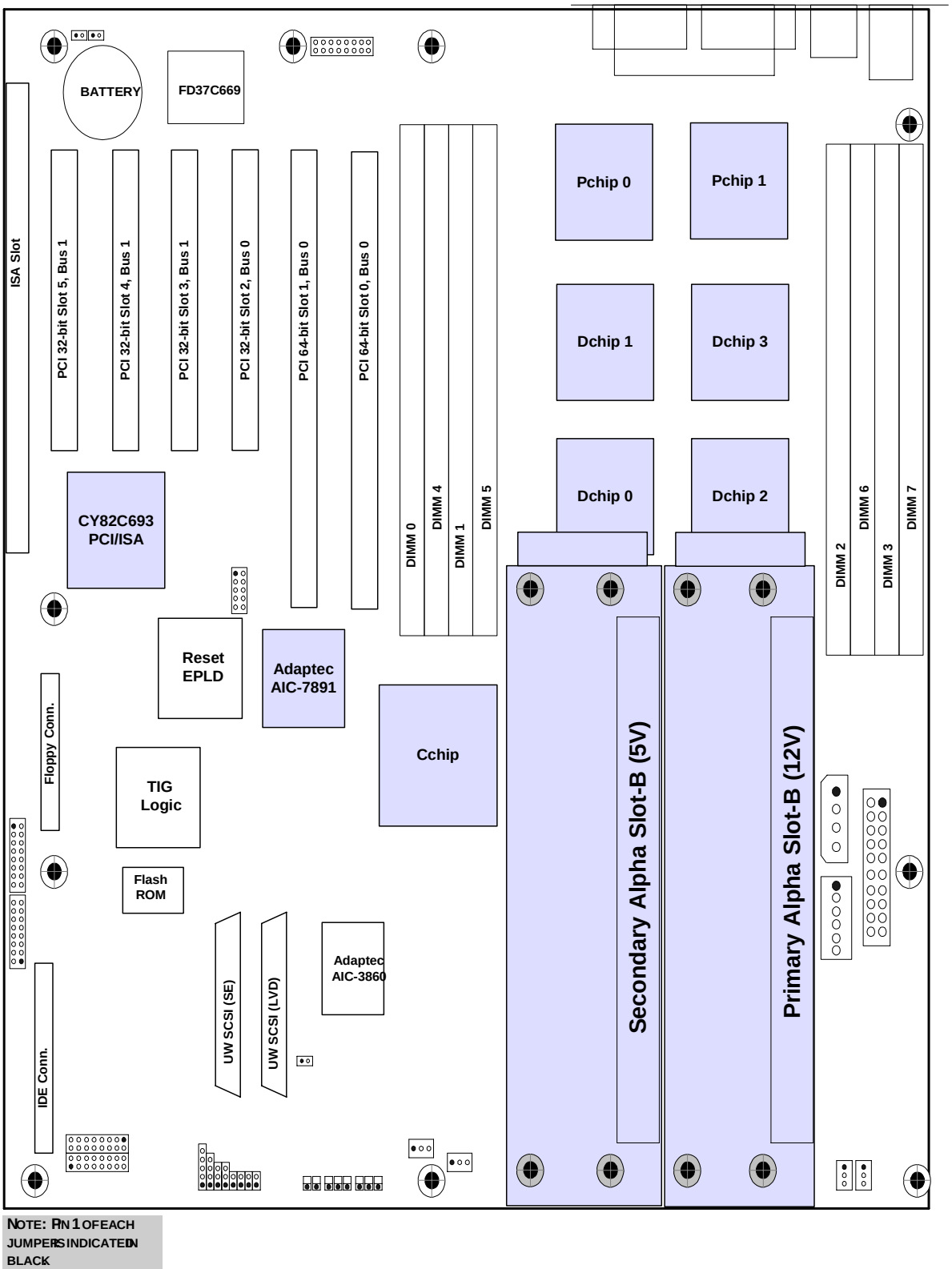


Figure 3-1 Thermally-sensitive Components

Table 3-5 Maximum Component Case Temperatures

Component	Maximum Temperature
Primary Alpha Slot B Module*	**<70°C (158°F)**
Secondary Alpha Slot B Module*	<64°C (147°F)
21272 D-chips	**<69°C (156°F)**
21272 P-chips	<66°C (151°F)
21272 C-chip	**<54°C (129°F)**
Adaptec AIC-7891 SCSI Controller	<69°C (156°F)
approved Southbridge peripheral bus controller	**<55°C (131°F)**

*Note: * Data from results of test using 667 MHz, 4 MB Alpha Slot B Modules. All other components' data from results of test using 750 MHz, 8 MB Alpha Slot B Modules.*

Thermal tests conducted by Alpha Processor, Inc. determined that these components remained within maximum specified temperatures. The test system configuration comprised the following:

- Dual 750 MHz, 8 MB Alpha Slot B Modules
- Fully-populated I/O and memory
- Minimum firmware to boot operating system (OS)
- 35°C ambient chamber

A thermocouple was placed on the base of each Alpha Slot B Module's heat sink, between the heat-sink mounting studs. All other components were instrumented at the top center of the case.

3.3 Enclosure Requirements

This product has been approved for use in either of following chassis:

- MACASE KA-S80FP chassis with AT-shaped power supply backplate, with the modification described in Application Note 51-0038-0A
- API CH320 3U Rack-mount Chassis

3.4 Physical Parameters

3.4.1 UP2000 Motherboard Parameters

The UP2000 Motherboard is a printed circuit board (PCB) with the dimensions specified in Table 3-6.

Table 3-6 UP2000 Motherboard Physical Parameters

Dimension	Value
Length	**330.2 mm (13 in)**
Width	304.8 mm (12 in)
Height	**1.6 mm (.06 in)**

3.4.2 Alpha Slot B Module Parameters

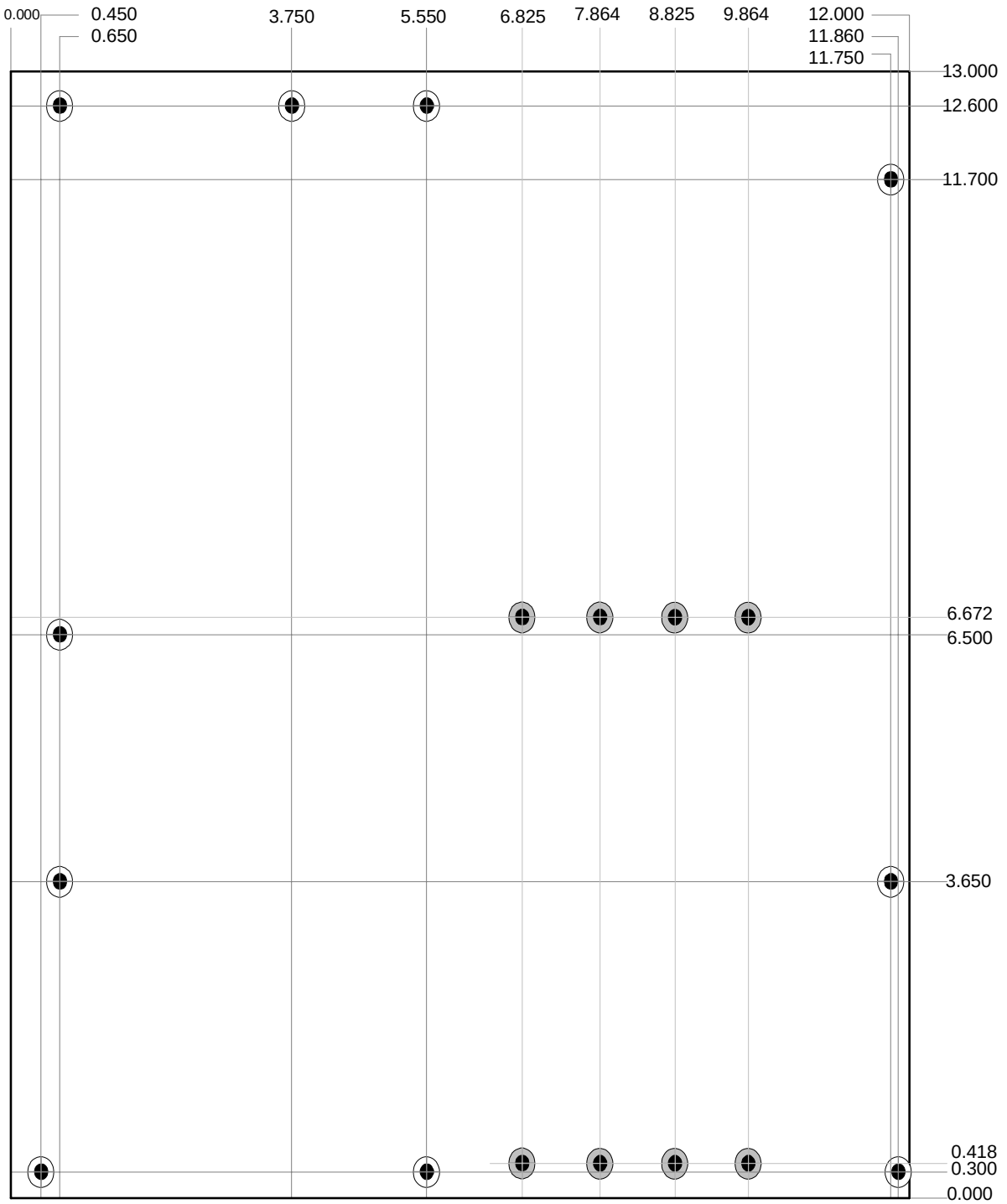
The Alpha Slot B Module is a PCB with the dimensions specified in Table 3-7.

Table 3-7 Alpha Slot B Module Physical Parameters

Dimension	Value
Length	**168.8 mm (6.6 in)**
Width	47.8 mm (1.9 in)
Height	**114.3 mm (4.5 in)**
Weight	**1.2 kg (2.6 lb)**

3.4.3 UP2000 Motherboard Mounting Hole Specification

The UP2000 Motherboard mounting hole specification is depicted in Figure 3-2.



Note: All values are in inches.

Figure 3-2 Mounting Hole Specifications

Chapter 4 Functional Description

This chapter describes the functional operation of the UP2000. It introduces the 21272 core logic chipset and briefly describes its implementation with the 21264 microprocessors.

Descriptions are also provided in this chapter of the subsystem structure of the UP2000, and the logic and firmware used.

4.1 21272 Core Logic Chipset

The UP2000 uses a Compaq 21272 (Tsunami) chipset to implement a uni-processor or dual-processor system based on the 21264 microprocessor, which is located on the Alpha Slot B Module. The chipset provides a 256-bit memory interface and includes the following three gate arrays:

- Cchip—controls address and commands, and is 432-pin Enhanced Super Ball Grid Array (ESBGA). The Cchip connects to the system interrupts by the TTL Integrated Glue Logic (TIG) block.
- Dchips—four 304-pin ESBGAs control the data path. Dchips provide the data path between the CPU, the memory and the Pchips.
- Pchips—two 304-pin ESBGAs control the PCI interface.

A 32-byte bus from the SDRAM arrays splits into two memory ports at the Dchips.

Refer to Compaq's documentation for a full explanation of the 21272 chipset.

4.1.1 Cchip Functional Overview

The Cchip provides the control interface between the Alpha Slot B Module, containing the 21264 microprocessor, and the UP2000 Motherboard 21272 chipset. In addition, it provides control for the Dchips, Pchips, memory subsystem and access to the TIG block.

The CPU and the Cchip communicate with each other through the system port. The system port is made up of unidirectional address and command buses. The Cchip system interface logic decodes the system port address for CPU requests to determine what action to take. It also decodes Direct Memory Access (DMA) requests.

The Cchip supports cacheable memory accesses, programmed I/O, interrupts, TIG addresses, and accesses to 21272 control/status register (CSR) space.

4.1.2 Dchip Functional Overview

The Dchips provide the data path from the 21264 to main memory. Four Dchips are used for the interface on the UP2000 Motherboard. The Dchips contain the CPU, Pchip, and memory interface data paths, which include DMA and Programmed Input/Output (PIO) queues.

The Dchips interface to the CPU using the CPU bus (sysdata). The CPU bus, between the Dchips and each CPU, passes 128 bits of data (64 bits, or 8 bytes, from each CPU).

There is also a 256-bit, bidirectional memory bus (memdata) between the Dchips and the memory banks. The memory bus connects to banks 0 and 1 (see Figure 4-4).

Dchips interface with each Pchip through the 32-bit I/O bus (padbus; padbus0 connects to Pchip 0 and padbus1 connects to Pchip 1). The I/O bus is a 32-bit data bus that allows a Pchip and the Dchips to pass data back and forth.

4.1.3 Pchip Functional Overview

The Pchip is a fully-compliant PCI host bridge between the PCI and the CPU and its cache and memory. Pchip interface protocol is compliant with *PCI Local Bus Specification, Revision 2.1*.

The Pchip contains all control functions of the PCI bridge and some data path functions. It acts as a master on the PCI for CPU-initiated transactions, and is a target on memory space transactions initiated by PCI masters. Two Pchips are used on the UP2000 Motherboard to provide one 64-bit PCI bus and one 32-bit PCI bus.

4.2 Subsystems

The following paragraphs describe the designs of the UP2000 functional subsystems.

4.2.1 Memory Subsystem

The UP2000 Motherboard has eight DIMM sockets arranged in two banks: bank 0 and bank 1. Each bank has four sockets and provides a 256-bit wide data path. DIMMs in the same bank must be the same type, size, and speed; DIMMs in different banks may differ in type, size, and speed. At least one memory bank must be filled for the UP2000 Motherboard to work.

The UP2000 supports memory DIMMs such as the sample list described in Table 4-1. This is not a comprehensive list of DIMMs supported.

Table 4-1 SDRAM DIMMs Supported

Vendor	Size	Vendor Part Number
Samsung	**64 MB**	**KMM350S823BT1**
	64 MB	KMM377S823BT1
	128 MB	**KMM377S1620BT1**
	256 MB	KMM377S3320T1
	256 MB	**KMM377S3323T**
	256 MB Stack	KMM377S3227BT1
Viking	**128 MB**	**PE16721R4SN3-2226**

4.2.2 CPU (Alpha Slot B Module) Interface

The UP2000 is designed to interface to one or two Alpha Slot B Modules. Two 330-pin connectors accept two Alpha Slot B Module connections for dual-21264 configuration. The board also works with a single Alpha Slot B Module connected, with the secondary Alpha Slot B Module connector left open.

Interface Connection

The Alpha Slot B Connector provides signal pins (154 total), 5 Volt pins (2A), 3.3 Volt pins (8A), 2V_TERM (58A), static RAM (SRAM) power pins (2A), and ground pins (70 total) from the UP2000 Motherboard. The VRM power source, connected on odd-numbered pins between 145–165, is auto-switched between 12V and 5V.

Alpha Slot B Module interface specifications are as follows:

- Molex part number: 74191-0002
- Designed for signal transmissions with rise and fall times of 0.5 nsec or greater

- Current rating: Signal contact = 1A, Ground contact = 1.5A

Bcache Subsystem

The external Bcache subsystem on the Alpha Slot B Module supports 2 MB, 4 MB or 8 MB cache sizes using a 128-bit data bus. Nine synchronous SRAMs (SSRAMs) are required per Alpha Slot B Module for 4 MB and 8 MB Bcache, and five SSRAMs are required per Alpha Slot B Module for 2 MB Bcache. Both Alpha Slot B Modules use late-write SSRAMs.

Note: *In a dual-processor system, the Bcache size must be the same for both Alpha Slot B Modules.*

The UP2000 supports Bcache using the SSRAM sizes shown in Table 4-2.

Table 4-2 Bcache Size

Bcache Size	SRAM Type
2 MB	**Four 128 K x 36 data SSRAMs and one 128 K x 36 tag SSRAM**
4 MB	Eight 256 K x 18 data SSRAMs and one 128 K x 36 tag SSRAM
8 MB	**Eight 512 K x 18 data SSRAMs and one 128 K x 36 tag SSRAM**

4.2.3 Clock Subsystem

The CPU and system clock frequency is decided by the UP2000 Motherboard's external PLL logic and the CPU internal PLL logic. The external PLL logic provides the reference clock input to the CPU and the 21272 chipset.

All external and internal PLL input parameters are set by TIG Field Programmable Gate Array (FPGA) logic configured by the UP2000 Motherboard CPU speed jumper (J34) and 21272 speed jumper (J29). This TIG FPGA has an internal PLL look-up table used to set the value of M[6:0] and N[1:0], which are input parameters of external PLL devices, and the value of Y-divider, which is an input parameter of CPU internal PLL logic.

These input values of the external PLL device are set through the TIG FPGA device using Inter-integrated Circuit (I2C) protocol.

Table 4-3 describes how the input parameters of external PLL are set.

Table 4-3 PLL Input Frequency

External PLL Output Freq.	M[6:0] Value	N[1:0] Value
83 MHz	**28h**	**10b**
133 MHz	20h	01b
150 MHz	**24h**	**01b**
166 MHz	28h	01b

The output frequency of this external PLL device is used as the CPU reference clock and system clock of the UP2000. The CPU reference clock produces the internal processor clock [GCLK] through internal PLL logic and the Y-divider value, which is multiplied as shown in Table 4-4.

Table 4-4 Reference Clock and CPU Clock for FID

FID Value	Max Speed	Used Speed	CPU_sp x TSU_sp x Y-Div	CLKin
00000	**500 MHz**	**500 MHz**	**3 x 4 x 3**	**166 MHz**
00010	600 MHz	600 MHz	4 x 1 x 4	150 MHz
00011	**666 MHz**	**666 MHz**	**5 x 4 x 4**	**166 MHz**
00101	750 MHz	750 MHz	6 x 1 x 5	150 MHz
00111	**866 MHz**	**833 MHz**	**6 x 4 x 5**	**166 MHz**
01000	933 MHz	900 MHz	7 x 1 x 6	150 MHz
01001	**1000 MHz**	**1000 MHz**	**7 x 4 x 6**	**166 MHz**

Note: The Y-divider value is set through IRQ[3:0] input signals and configured by the TIG FPGA internal PLL look-up table, with the CPU speed jumper and the 21272 speed jumper.

The PLL look-up table for the UP2000 is shown in Table 4-5. The value of the column Flash Select Jumper indicates one among eight established Reset PAL codes for the Alpha Slot B Module.

Table 4-5 System Clock and 21272 Operating Frequency

Setting Jumper			MC439 Input Val		IRQ[3:0]	Operating Frequency (MHz)		
CPU Spd (J34)	21272 Spd (J29)	Flash Select (J34)	M[6:0] Value (Dec)	N[1:0] Value (Dec)	Y-Div Value	CLKIN (To CPU)	CPU Clock (GCLK)	System Clock
3 (011)	**4**	**7**	**40**	**1**	**3**	**166**	**500**	**83**
4 (100)	1	0	36	1	4	150	600	75
5 (101)	**4**	**1**	**40**	**1**	**4**	**166**	**667**	**83**
	4	6	40	1	7	166	1162	83
6 (110)	**1**	**2**	**36**	**1**	**5**	**150**	**750**	**75**
	4	3	40	1	5	166	833	83
7 (111)	**1**	**4**	**36**	**1**	**6**	**150**	**900**	**75**
	4	5	40	1	6	166	1000	83

The CPU and system clock design is shown in block diagram form in Figure 4-1.

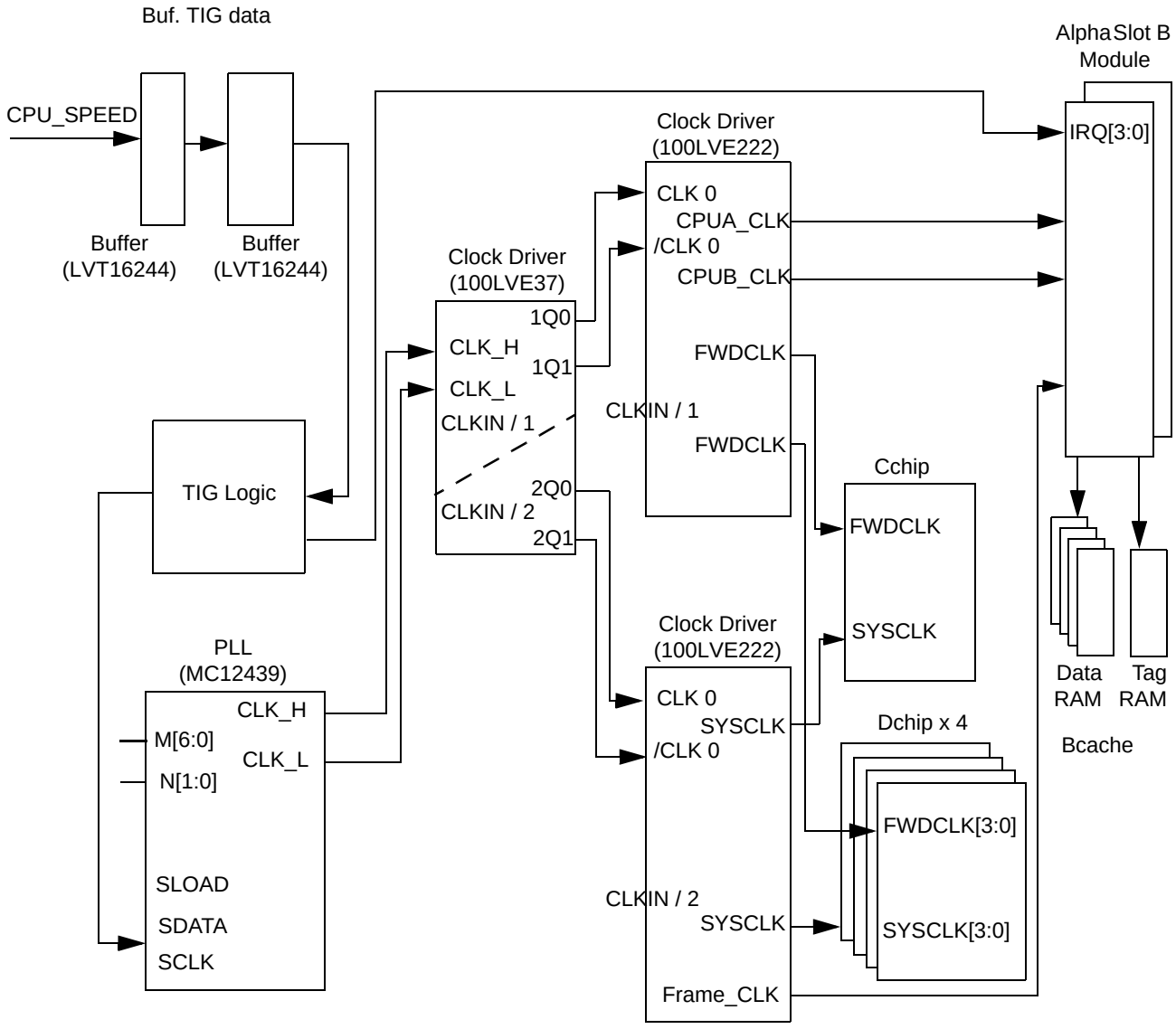


Figure 4-1 CPU and System Clock Block Diagram

The LVE37 clock driver receives PLL clock signals, and performs an x 1 or x ½ operation and sends the output to the LVE222 clock driver (1:15 differential x 1 or x ½). The x 1 clock is sent to LVE222 for the CPU clock and for the forward clock drive for each chipset, and x ½ clock is sent to the other LVE222 for system clock for each chipset.

Memory Interface Clock

The low voltage PLL clock driver (MPC951), which received system clock through the clock drive, goes through each DIMM as 1:1 clock output. One clock is used as a feedback clock to reduce the skew.

There are a total of nine clock outputs. Since the 168-pin DIMM used in the

UP2000 is registered (including PLL), only one clock source is needed to do the loading.

Figure 4-2 shows a block diagram of the UP2000 memory interface clock design.

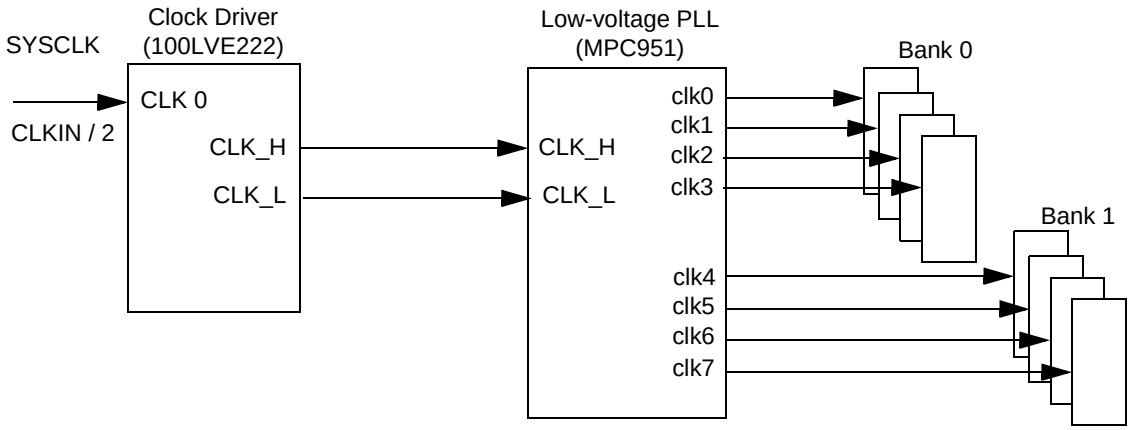


Figure 4-2 Memory Interface Clock Block Diagram

PCI Clock

The set value of the internal register PCLKX determines which divide ratio the Pchips use for dividing the forward clock signal. Refer to Table 4-6 for a list of the divide ratio values.

Table 4-6 PCI Clock Frequency Multiplier

PCLKX	Forward Clk Divide Ratio
0	**6**
1	4
2	**5**

Pchip register PCTL contains PCLKX[41:40], which can be used to configure the PCI clock frequency multiplier.

The PCLKX value is set in the Reset PAL code. The value is used when the Reset PAL code starts initializing the Pchip when the code goes into the Icache (instruction cache) of the CPU.

Refer to Figure 4-3 for a block diagram of the PCI clock design.

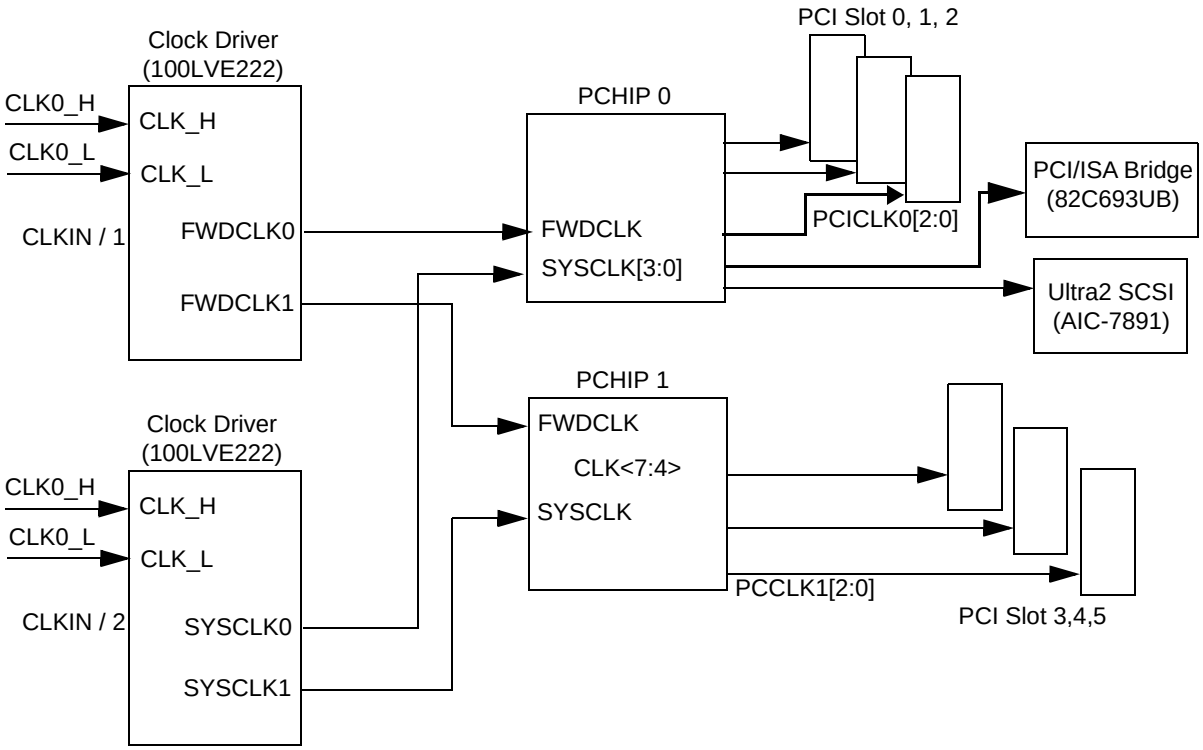


Figure 4-3 PCI Clock Generation Block Diagram

4.2.4 System Bus

The clock speed of the bus between the CPU and the chipsets is set up as 83 MHz.

The maximum bandwidth is designed as 2.67 GBytes/second. The bus between CPU and Dchips is designed as a 64-data bit bus, and the bus between Dchips and memory is designed as a 1-bus, 2-bank, and 32-byte bus.

Figure 4-4 shows a block diagram of the system bus design.

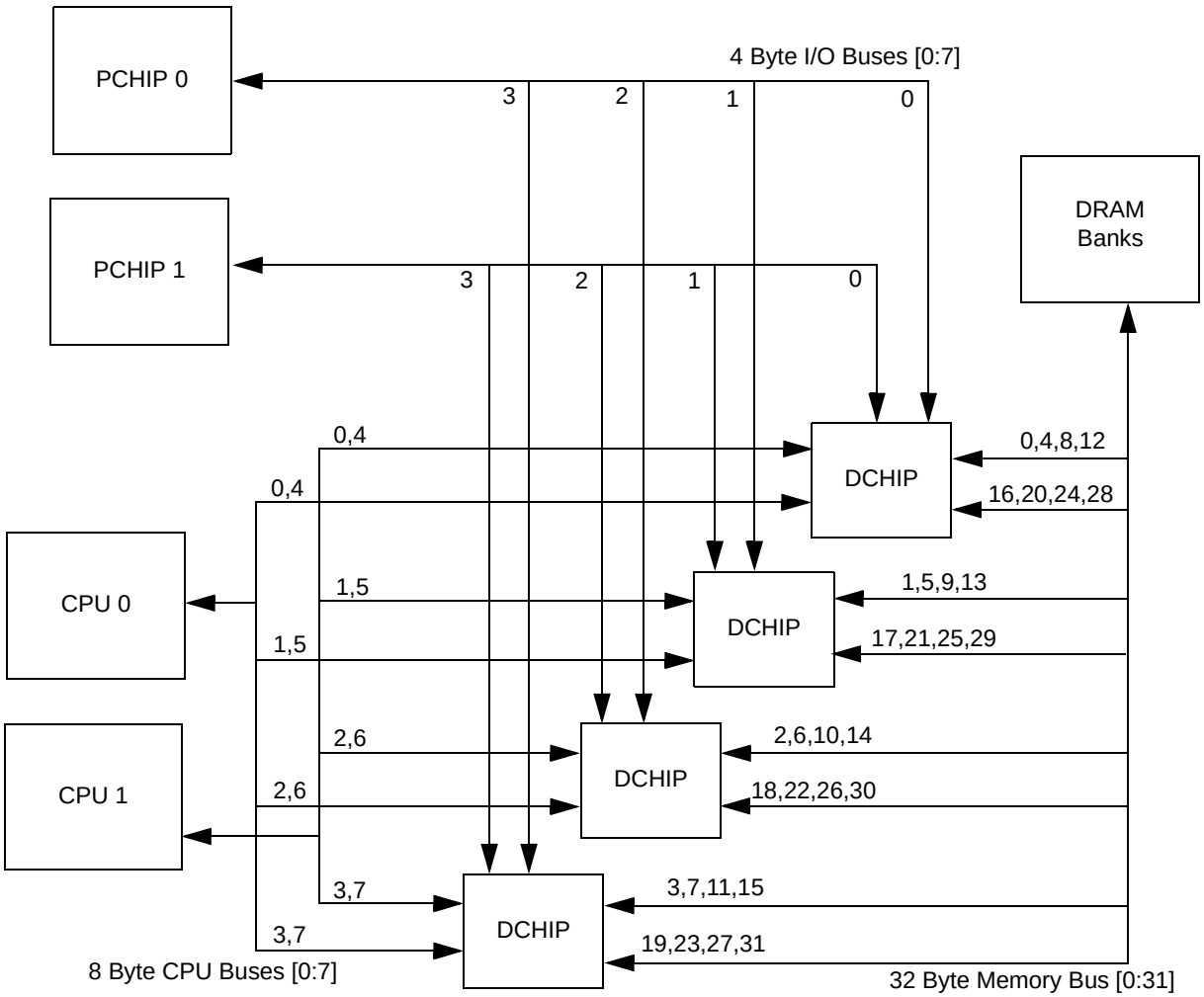


Figure 4-4 System Bus Block Diagram

The UP2000 has two CPU buses with an 8-byte data width, and one memory bus with a 32-byte data width. This is accomplished by using one Cchip, four Dchips and two Pchips. Each of the dynamic RAM (DRAM) banks is split into two memory ports of the Dchips. A cache block is read or written to the memory using two transfers on this bus. Each Dchip supplies two bytes to each installed CPU.

The instantaneous peak data transfer rates between the Dchips and the DRAM bank is 32 Bytes at 83 MHz, which is equal to 2.67 GB/sec. The instantaneous peak transfer rates between the CPUs and Dchips is 8 Bytes at 333 MHz (that is, a 167 MHz, double data rate), which is also equal to 2.67 GB/sec. The interface between Pchips and Dchips is 4 bytes at 83.3 MHz, which results in an instantaneous peak data transfer rate of 333 MB/sec.

4.2.5 PCI Interface

The UP2000 supports six PCI slots (two 64-bit and four 32-bit) and one shared PCI/ISA slot. The PCI interface has a 33 MHz system clock. The UP2000 also provides a PCI-to-ISA bridge (CY82C693UB). The on-board AIC-7891 has up to 80 MB/sec data transfer rates and a 64-bit PCI interface.

The primary Pchip is connected to the CY82C693UB PCI/ISA bridge, the Ultra2 SCSI Controller (AIC-7891), two 64-bit PCI slots, and one 32-bit PCI slot.

The secondary Pchip is connected to three 32-bit PCI slots.

Primary PCI Bus

The primary PCI bus (bus 0) has the following interconnections, as described in Table 4-7 and Table 4-8:

- Two 64-bit, 5V PCI slots
- One 32-bit, 5V PCI slot
- One CY82C693UB PCI/ISA bridge interface
- One AIC-7891 Ultra2 SCSI controller interface

Table 4-7 PCI 0 Configuration ID

IDSEL Value	Device
AD16	**CY82C693UB**
AD17	AIC-7891
AD18	**PCI Slot 0**
AD19	PCI Slot 1
AD20	**PCI Slot 2**

Table 4-8 Primary PCI Arbitration

Arbitration Signals	Device Connected
P_REQ0#/P_GNT0#	**CY82C693UB**
P_REQ1#/P_GNT1#	AIC-7891
P_REQ2#/P_GNT2#	**PCI Slot 0**
P_REQ3#/P_GNT3#	PCI Slot 1
P_REQ4#/P_GNT4#	**PCI Slot 2**

Secondary PCI Bus

The secondary PCI bus (bus 1) has three 32-bit, 5V PCI slots, as described in Table 4-9 and Table 4-10.

Table 4-9 PCI 1 Configuration ID

IDSEL Value	Device
AD18	**PCI Slot 3**
AD19	PCI Slot 4
AD20	**PCI Slot 5**

Table 4-10 Secondary PCI Arbitration

Arbitration Signals	Device Connected
P_REQ0#/P_GNT0#	**PCI Slot 3**
P_REQ1#/P_GNT1#	PCI Slot 4
P_REQ2#/P_GNT2#	**PCI Slot 5**
P_REQ4#/P_GNT4#	Not Used

4.2.6 On-Board I/O

The on-board I/O provided on the UP2000 Motherboard are defined in Table 4-11.

Table 4-11 On-board I/Os

I/O Component	Specification
FDC37C669	• **2.88 MB floppy disk controller**
	• Two Serial ports, NS16C550 compatible
	• **One Parallel port**

Table 4-11 On-board I/Os (Continued)

I/O Component	Specification
CY82C693UB	• PCI-to-ISA bridge, *PCI Local Bus Specification Revision 2.1* compliant
	• **DMA controllers with type A, B, and F support**
	• Interrupt controllers
	• **Timer/counters**
	• Real-time clock with 256 bytes of battery-backed SRAM
	• **Dual-channel, EIDE controller with PCI bus mastering, CD-ROM support, PIO modes 0 through 4 operation, and single-word and multi-word DMA modes 0 through 2**
	• Keyboard and mouse controller
	• **PCI-ISA/ISA-PCI/IDE-PCI/PCI-IDE post writing**
	• USB controller
	• **Two USB ports**
AIC-7891 (SCSI Controller)	• Supports Ultra2 LVD devices with 80 Mbyte / sec data transfer rate in 16-bit mode or 40 MByte / sec in 8-bit mode.
	• **Supports single-ended SCSI devices with an additional driver IC, AIC-3860**
	• 512-byte data First In, First Out (FIFO) buffer for efficient PCI bus utilization
	• **PCI-tagged command queuing allows changes in the order of SCSI command execution**
	• Connection for up to 15 SCSI devices on 12 meter cable

Refer to Figure 4-5 for a block diagram of the SCSI controller design.

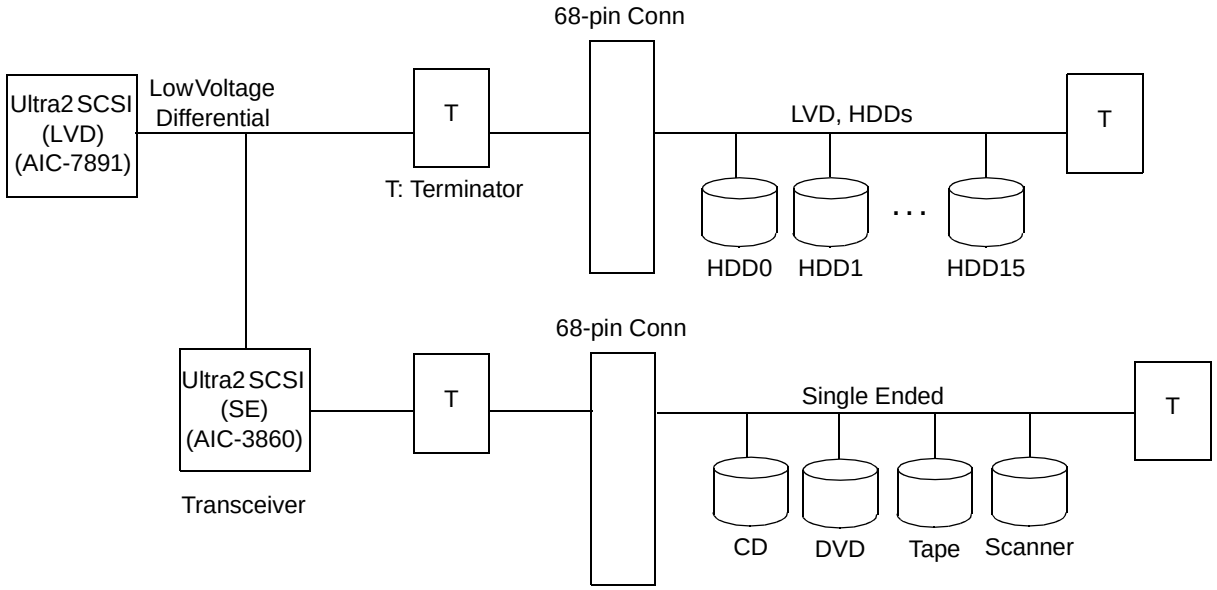


Figure 4-5 SCSI Controller Block Diagram

4.3 Logic

4.3.1 CPU Speed Logic

The CPU speed is set by the Y-divider value, FID[3:0], sent on the initial IRQH signal input through the interrupt bus, which resulted from the combination of CPU speed and the 21272 speed input to the Reset EPLD from configuration jumper J34.

The UP2000 supports only same-speed CPUs on both processors. CPU speed is determined by configuration jumper J34 on the UP2000 Motherboard. Refer to Figure 2-3 on page 2-7 for details.

A diagram of the CPU speed logic is shown in Figure 4-6.

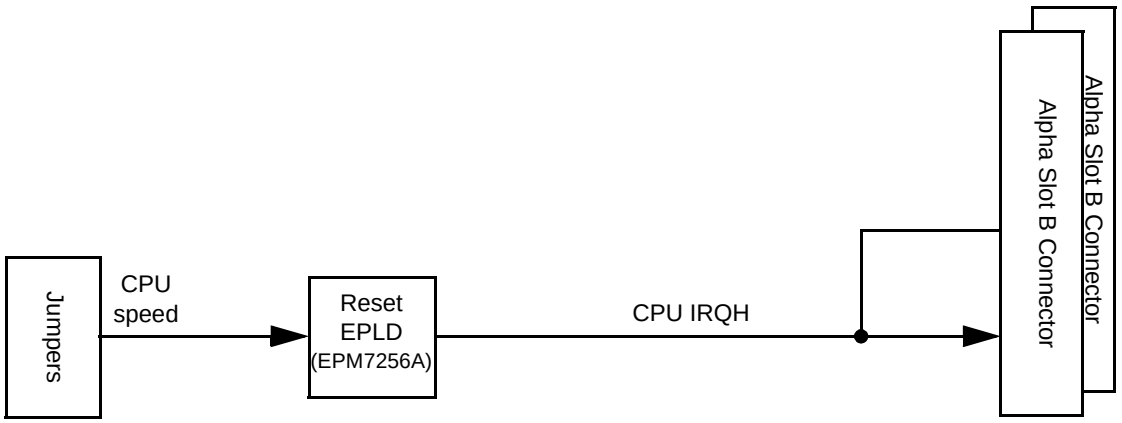


Figure 4-6 CPU Speed Logic

4.3.2 Interrupt Logic

The TIG FPGA decoder divides a total of 64 interrupt sources by eight, then transfers them through the TIGbus.

The UP2000 receives the thermal sensor interrupt signal I2C_INTR_L from each Alpha Slot B Connector, and uses a flip-flop design to support the interrupt even if only one interrupt is received.

The UP2000 was designed to support only one on-board SCSI controller interrupt. It uses the AIC-7891, which supports one LVD port, and the AIC3860, which supports one single-ended port.

A block diagram of the interrupt logic design is shown in Figure 4-7. Table 4-12 provides a map of the UP2000 logical interrupts.

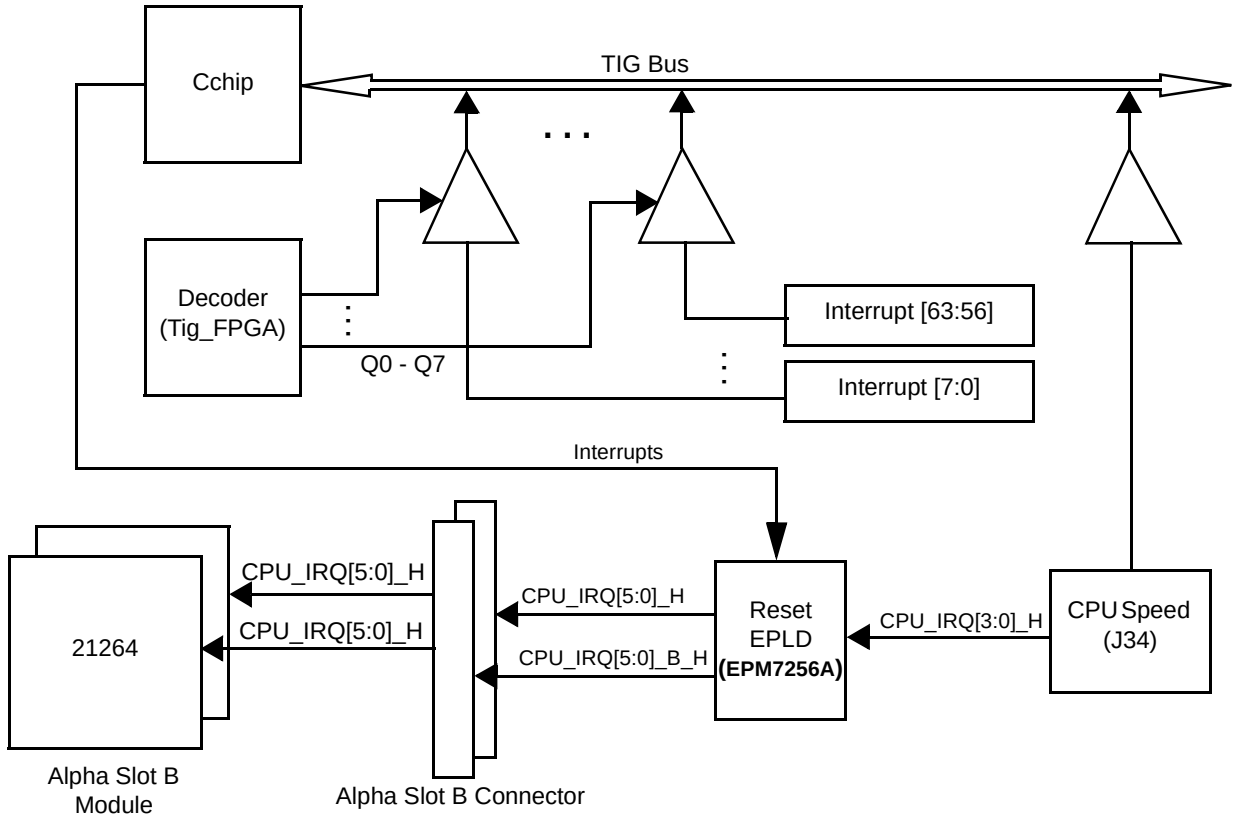


Figure 4-7 Interrupt Logic Block Diagram

Table 4-12 Logical Interrupt Map

INT_EN	Interrupt Level	Signal Name
INT_EN0	**16**	**Reserved**
	17	I2C_INT I2C Controller (PCF8584)
	18	**Reserved**
	19	PCI0_IRQ_ADPTA
	20	**PCI0_INTD2**
	21	PCI0_INTC2
	22	**PCI0_INTB2**
	23	PCI0_INTA2

Table 4-12 Logical Interrupt Map (Continued)

INT_EN	Interrupt Level	Signal Name
INT_EN1	**24**	**PCI0_INTD1**
	25	PCI0_INTC1
	26	**PCI0_INTB1**
	27	PCI0_INTA1
	28	**PCI0_INTD0**
	29	PCI0_INTC0
	30	**PCI0_INTB0**
	31	PCI0_INTA0
INT_EN2	**32**	**PCI1_INTD3**
	33	PCI1_INTC3
	34	**PCI1_INTB3**
	35	PCI1_INTA3
	36	**PCI1_INTD2**
	37	PCI1_INTC2
	38	**PCI1_INTB2**
	39	PCI1_INTA2
INT_EN3	**40**	**PCI1_INTD0**
	41	PCI1_INTC0
	42	**PCI1_INTB0**
	43	PCI1_INTA0
	44	**PCI1_INTD1**
	45	PCI1_INTC1
	46	**PCI1_INTB1**
	47	PCI1_INTA1
INT_EN4	**48**	**Reserved**
	49	Reserved
	50	**THERM_WARN (Alpha Slot B Module Thermal Interrupts)**
	51	Reserved
	52	**Reserved**
	53	CYP_NMI
	54	**SMI_INT**
	55	ISA_INT

Table 4-12 Logical Interrupt Map (Continued)

INT_EN	Interrupt Level	Signal Name
INT_EN5	**56**	**Reserved**
	57	Reserved
	58	**Reserved**
	59	Reserved
	60	**Reserved**
	61	PCI1_ERROR
	62	**PCI0_ERROR**
	63	Reserved

4.3.3 Reset PAL Code Access Logic

Reset EPLD supplies the Reset PAL code data to initialize the CPUs at reset. Settings on J34 on the UP2000 Motherboard configure a flash select value (see Table 2-2 on page 2-6). This flash select value determines which of the eight Reset PAL code images stored in flash ROM is sent to the CPU. The CPU holds the Reset PAL code output enable signal until the data load is complete.

Reset EPLD performs the following steps to load each CPU:

1. Dcok_A_H becomes active with Power_on_reset.
2. After Dcok_A_H is input, CPU0 holds about 8 GCLK cycles and the real EV6CLK_x cycle occurs.
3. The Reset EPLD receives Mod_reset, then sends Real_reset_A_L to the CPU.
4. The CPU0 which receives Real_reset_A_L finishes the PLL setting and enables Srom_En_A_L.
5. The Reset EPLD which receives Srom_En_A_L checks whether CPU1 is present.
   - If one CPU is used (CPU0 only):
     a. Reset EPLD bypasses Srom_En_A_L and sends the signal to the Cchip.
     b. When the Cchip receives this signal, it enables ClkFwdRst_H.
     c. The CPU which received ClkFwdRst_H performs Built-in Self Test (BIST), and loads SROM_Data into the CPU Icache.
     d. After loading SROM_Data, the CPU deasserts Srom_En_L.
     e. The Cchip checks this signal, and finishes it by deasserting ClkFwdRst_H.
   - If two CPUs are used (CPU0 and CPU1):

a. After Srom_En_A_L is input, SROM_Data finishes loading into the Icache of CPU0, and Srom_En_A_L is deasserted. This Srom_En_A_L signal is latched so that the enabled signal goes into the Cchip.
b. When Srom_En_A_L is deasserted in the Reset EPLD internally, it enables Dcok_B_H and Real_reset_B_L.
c. When Srom_En_B_L goes into Reset EPLD after being enabled, the Reset EPLD bypasses the signal and sends it to the Cchip.
d. At this time, Reset EPLD deasserts the Real_reset_B_L which is latched. This causes both CPUs to enter RUN mode (that is, the execution of Reset PAL code data) at the same time by receiving ClkFwdRst_H from the Cchip.

In other words, Reset EPLD receives Srom_En_L of the primary Alpha Slot B Module and maintains the signal low until the Reset PAL code data gets loaded into the Icache of the secondary Alpha Slot B Module. After Reset PAL code data is finished loading by both Alpha Slot B Modules, Srom_En_L is deasserted in both Alpha Slot B Modules at the same time to initialize the CPUs.

Reset EPLD is an ALTERA EPM7256A, 144-Pin ISP type component. Input Clock uses the CY2081 output clock of 14.318 MHz.

Figure 4-8 provides a diagram of the Rest PAL code access logic design used in the UP2000.

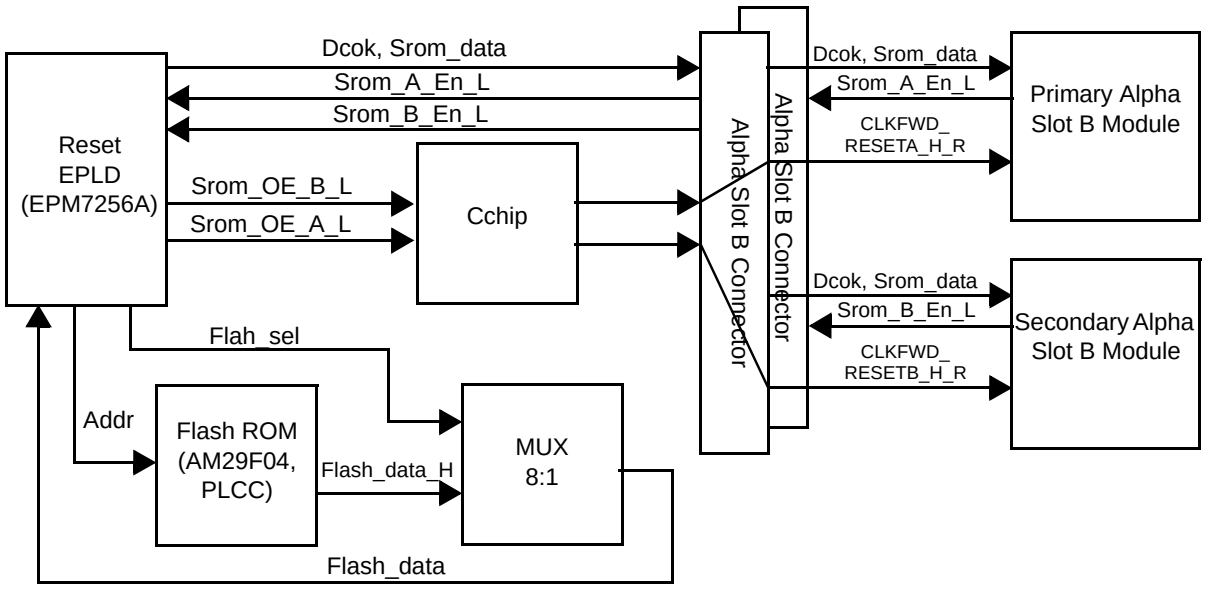


Figure 4-8 Reset PAL Code Access Logic

4.3.4 Fan Connector Logic

Each Alpha Slot B Module supports two fans, resulting in the use of a total of four fans and four fan connectors. On the UP2000 Motherboard, each slot's FAN_OK signal goes through a logical AND gate in Reset EPLD. If all four fans function normally, the CPU_Dcok signal is asserted to the CPU.

4.3.5 On-board LED Logic

Six LEDs are used to indicate the status of the SROM_CLK, DC_OK, and 2V PWRGOOD signals on both the primary and secondary Alpha Slot B Modules. Two LEDs are used to indicate signal activity for the SCLK and SDATA clock generator configuration signals.

Figure 4-9 provides a diagram of the LED locations. All eight LEDs are located on the front edge of the UP2000 Motherboard, to the left of the secondary Alpha Slot B Module. Table 4-13 describes the LED functions.

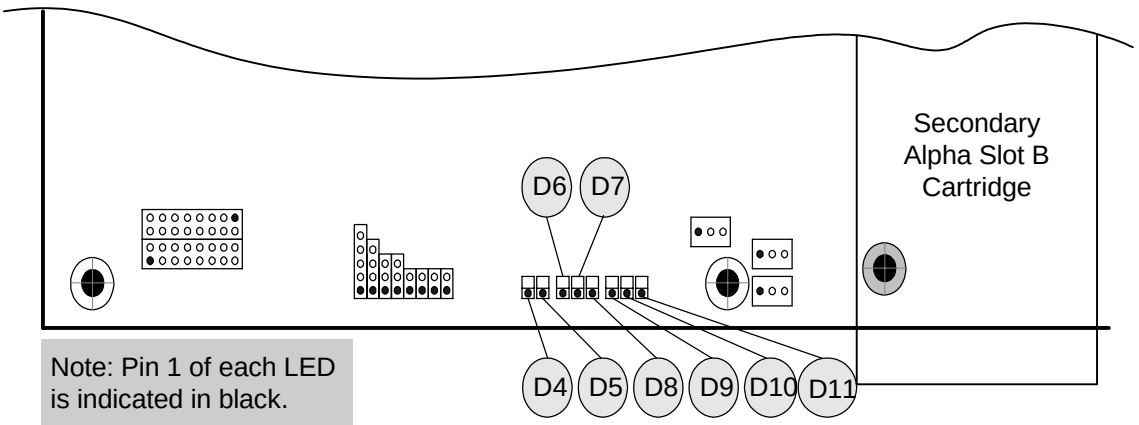


Figure 4-9 LED Locations

Table 4-13 LED Functions

LED	Function
D4	**SCLK_L for clock generator configuration**
D5	SDATA_L for clock generator configuration
D6	**Secondary Alpha Slot B Module DC_OK**

Table 4-13 LED Functions

LED	Function
D7	Secondary Alpha Slot B Module SROM_CLK
D8	**Secondary Alpha Slot B Module PWRGOOD**
D9	Primary Alpha Slot B Module DC_OK
D10	**Primary Alpha Slot B Module SROM_CLK**
D11	Primary Alpha Slot B Module PWRGOOD

4.3.6 Alpha Slot B Connector Logic

Both Alpha Slot B Connectors use a 330-pin Molex connector, designed to support 12V and 5V. The primary Alpha Slot B Connector is hardwired with 12V and the secondary Alpha Slot B Connector is hardwired with 5V.

4.3.7 Reset Logic

The UP2000 reset logic starts from the Power OK signal of the power supply. The processor reset starts from the Alpha Slot B Module reset FPGA logic. System reset and peripheral I/O reset signals are derived from the Cchip as shown in Figures 4-10 and 4-11.

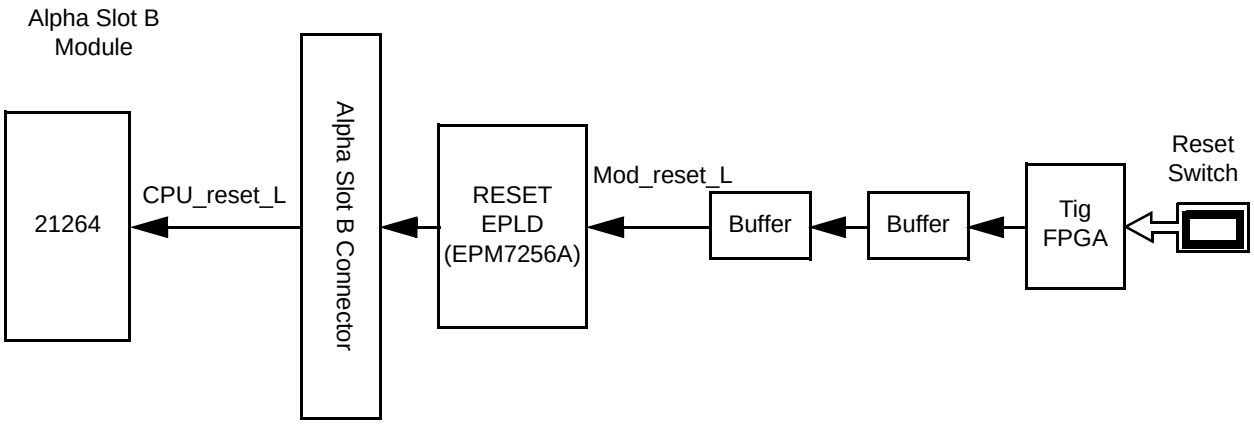


Figure 4-10 Alpha Slot B Module Reset Logic

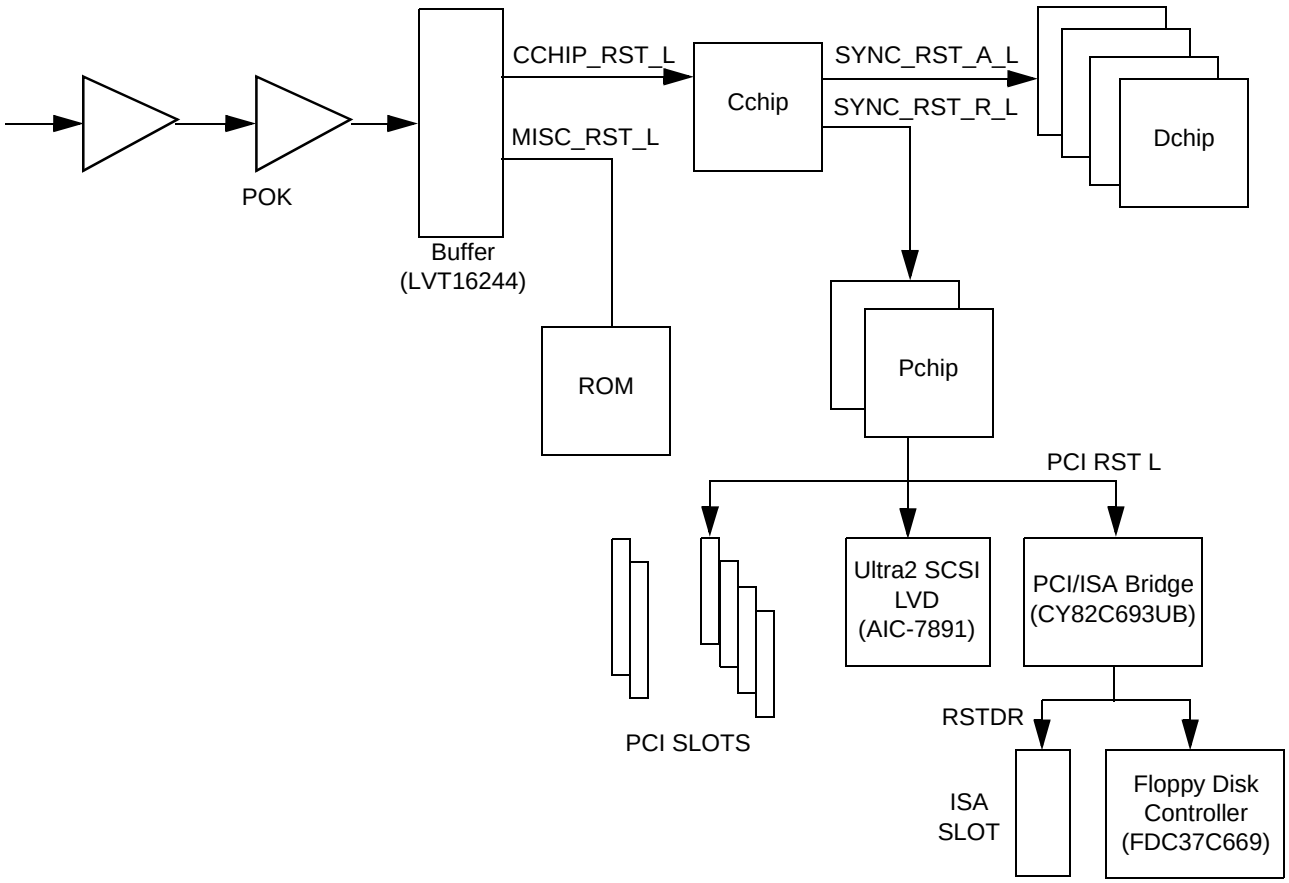


Figure 4-11 System Reset Logic

4.3.8 I2C Logic

The I2C controller (PCF8584) changes serial I2C data from the Alpha Slot B Modules to parallel signals, then sends them to the PCI/ISA bridge interface. The UP2000 also supports the memory DIMM I2C data from the I2C controller in the PCI/ISA bridge interface.

Table 4-14 shows the address mapping of the PCF8582C I2C EPROM and the LM75CIM3 thermal sensor. Figure 4-12 provides a diagram of the I2C Bus logic used in the UP2000.

Table 4-14 I2C Address Map

Component	Primary Alpha Slot B Module	Secondary Alpha Slot B Module	Memory Bank 0	Memory Bank 1	On-board
PIO PCF8582C	**1010010**	**1010110**			**1010001**
PIO LM75CIM3 thermal sensor	1001010	1001110			
Cchip			**000**	**100**	

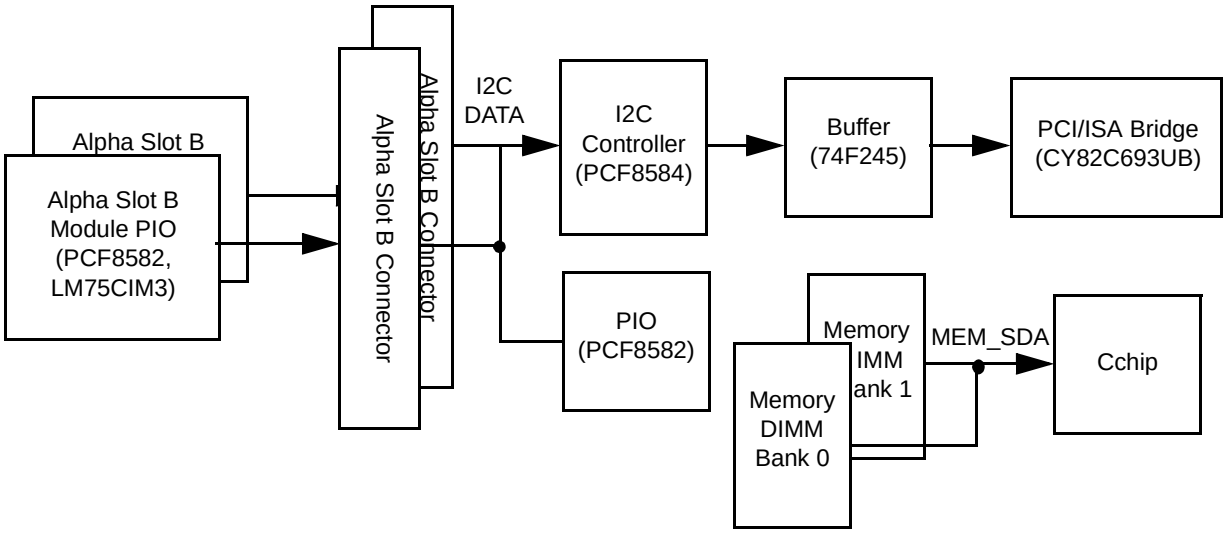


Figure 4-12 I2C Bus Logic

4.4 Firmware

This section describes the UP2000 target operating system (OS), and the Reset PALcode, Alpha Diagnostics, and Alpha SRM console firmware. A description is included of the order in which firmware loads.

The UP2000 supports the following firmware versions:

- Reset PALcode (SROM code)—version 1.9.3 or higher
- Alpha Diagnostics—version 1.1 or higher
- Alpha SRM Console—version A5.5-82 or higher

4.4.1 Supported OS

The UP2000 supports Linux kernels 2.2.13 or later.

Note: *Refer to product support at the Alpha Processor, Inc. web site for current information on specific distributors and OS versions supported by the UP2000.*

4.4.2 Reset PAL Code

When the UP2000 is turned on or reset, Reset PALcode automatically loads into Icache in the CPU. This Reset PALcode performs the following:

1. Initialize CPU.
2. Initialize CSR values—memory timing, Cchip, Dchip, and Pchip values.
3. Detect configuration jumpers, CPU configuration setting, and memory.
4. Initialize Bcache and set core logic chipset CSRs according to configuration.

   Note: *In the 21272 chipset, there are 23 CSRs for the Cchip, 4 CSRs for the Dchips, and 48 CSRs for the Pchips.*

5. Initialize system memory.
6. Detect CPU speed by polling of Periodic Interrupt Flag in the RTC.
7. Load the next level of firmware and pass control to that code. (See section 4.4.5, “Firmware Loading Order.")

Each Alpha Slot B Module requires a specific Reset PALcode image, depending on the CPU speed. CPU speed is supplied by the FID value determined by the Alpha Slot B Module.

Note: *If you use two Alpha Slot B Modules, both modules must use the same CPU speed. This means that both Alpha Slot B Modules also use the same Reset PALcode.*

4.4.3 Alpha Diagnostics

The Alpha Diagnostics firmware is used internally by Alpha Processor, Inc. for diagnostic purposes.

Native mode diagnostics depends on various system components to be functioning correctly. When Reset PALcode determines that the UP2000 is capable of supporting the higher level environment, it fetches this image from the firmware and transfers control to it.

An Alpha Slot B Module using an 21264 processor implements a serial communications link directly connected to the processor. This link, called

the Debug Port, can be used for reporting and interacting in the earliest stages of system initialization, after execution passes from PAL mode. It is accessed through J43 (primary) or J42 (secondary) on the UP2000 Motherboard (see Figure 2-1 on page 2-2).

The Alpha Diagnostics firmware includes the following tests:

- Interrupt handling—Raise interrupts with a known response
- UP2000 Motherboard components—chipset, Flash ROM integrity, on-board devices
- Memory—stress test
- ISA cards
- PCI bus—Initialization, stressing and interrupts
- SM timer support and EEPROMs
- FDD and IDE disks—DMA

If the Alpha Diagnostics detects a working keyboard and video console, it displays a graphical interface containing a menu of diagnostics. This is the console interface to the Alpha Diagnostics. If the Alpha Diagnostics does not detect a video console, the Alpha Diagnostics uses the Debug Port interface.

4.4.4 Alpha SRM Console

The Alpha SRM Console firmware provides service functions commonly provided in most computers systems, including the following:

- Power-up diagnostics and initialization
- Operator interface
- OS bootstrap and restart

Alpha SRM Console firmware provides SRM support for Linux and for booting the firmware update image.

Users (operators) communicate with the SRM Console through a system console device. SRM Console firmware supports the use of either of the following:

- VT-style terminal attached to the standard serial port
- Standard VGA monitor and keyboard

SRM Console firmware provides a command line interface (CLI), or command shell. It supports both a scripting facility and one of two shells. The shell is either a simple shell for single-command line execution, or a UNIX-style shell (a subset of a Bourne shell) providing a rich set of commands and operators.

4.4.5 Firmware Loading Order

UP2000 firmware loads in the following order:

1. Load Reset PALcode firmware.
   - If system firmware is corrupted, load Alpha Diagnostics. See 2.2.1, “Diagnostics and Flash Recovery,” on page 2-5 for information on Alpha Diagnostics.
   - When Reset PALcode firmware is loaded, go to step 2.
2. Check for configuration to enable Alpha Diagnostics.
   - If enabled, load Alpha Diagnostics. See 2.2.1, “Diagnostics and Flash Recovery,” on page 2-5 for information on Alpha Diagnostics.
   - If Alpha Diagnostics is not enabled, go to step 3.
3. Load Alpha SRM console.

   SRM loads and runs the Linux kernel and its PALcode.

Chapter 5 System Memory and Address Mapping

The following sections describe the UP2000 system memory, and includes a list of valid memory configurations. Mapping information for system addresses is also provided.

5.1 Memory Subsystem

The UP2000 has eight DIMM sockets arranged in two banks: bank 0 and bank 1. Each bank has four sockets and provides a 256-bit wide data path.

The minimum memory size is 256 MB (four 64 MB DIMMs), and the maximum size is 2 GB (eight 256 MB DIMMs). When the system clock is 83.3 MHz, the maximum bandwidth becomes 2.67 GB/sec. System firmware automatically detects memory type and size.

The UP2000 supports the following:

- 168-pin, 100 MHz SDRAM, PLL or registered SPD DIMMs
- LVTTL-compatible inputs and outputs
- 3.3V +- 0.3V power supply

Each 168-pin DIMM should have eight Data Input/Output Mast (DQM) signals for each DIMM. Because there is no guarantee of all 32 loadings with DQM from the Cchip, API uses a 200 psec Quick switch, part number PI3B3244, as shown in Figure 5-1.

Note: *DIMMs installed in one memory bank must be of the same type, size and speed. DIMMs installed in different memory banks may differ between banks, but not within a bank.*

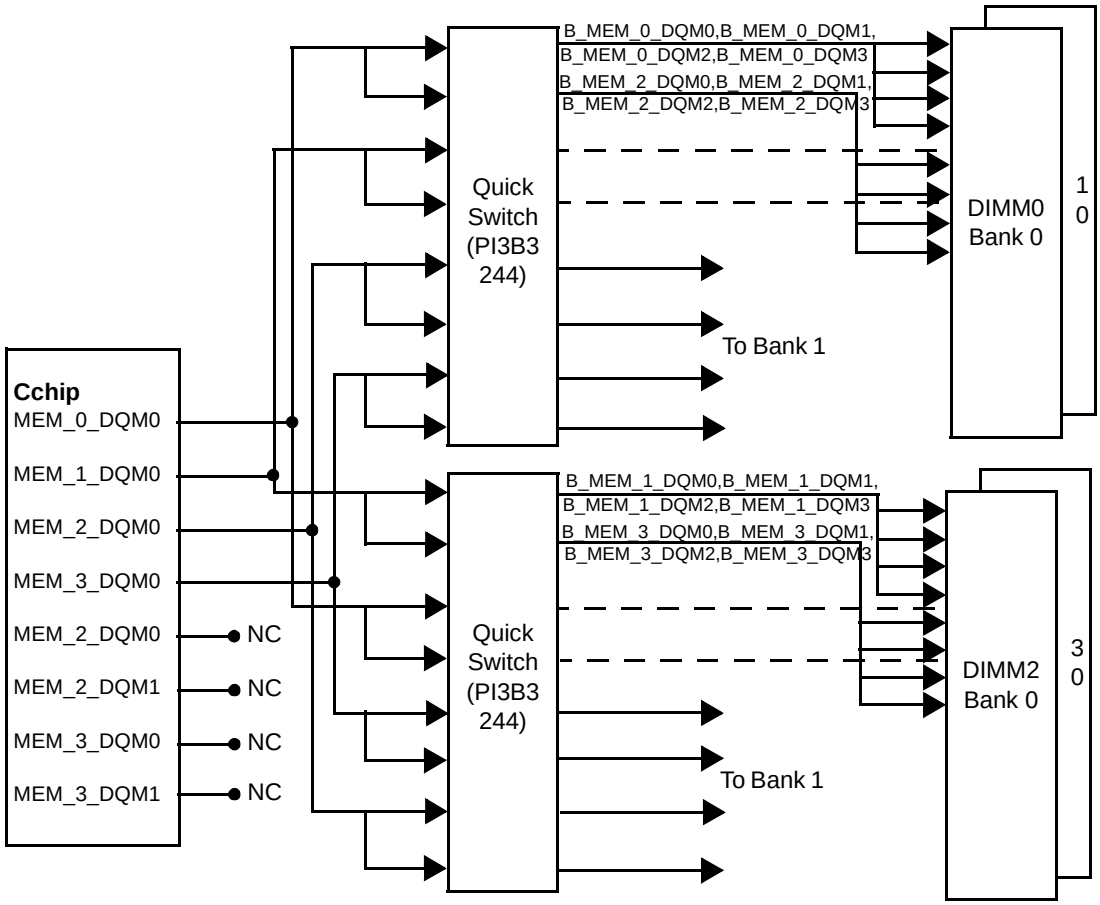


Figure 5-1 Memory DQM Configuration

5.2 Configuring SDRAM Memory

The UP2000 supports memory sizes from 256 MB to 2 GB. Table 5-1 lists some of the SDRAM memory configurations available. Any combination of DIMMs that meet the 21272 configuration rules are supported by the 21272 chipset.

For a list of vendors who supply components and accessories for the UP2000, see Appendix B.

Table 5-1 UP2000 SDRAM Memory Configurations

Total Memory	Bank 0	Bank 1
256 MB	**64 MB x 4**	
512 MB	128 MB x 4	
	64 MB x 4	**64 MB x 4**
768 MB	128 MB x 4	64 MB x 4
1 GB	**256 MB x 4**	
	128 MB x 4	128 MB x 4
1.5 GB	**256 MB x 4**	**128 MB x 4**
2 GB	256 MB x 4	256 MB x 4

5.3 System Address Mapping

This section describes the mapping of the processor physical address space into memory and I/O space addresses. It also includes the translations of the processor-initiated address into a PCI address, and PCI-initiated addresses into physical memory addresses.

5.3.1 CPU Address Mapping to PCI Space

The physical CPU bus address space is composed of the following:

- Memory address space
- Local I/O space for registers in the Cchip, Dchips, and Pchips)
- PCI space

The PCI defines four physical address spaces, as follows:

- PCI memory space (for memory residing on the PCI)
- PCI I/O space
- PCI configuration space
- PCI interrupt acknowledge cycles/PCI special cycles

Refer to Compaq's functional specification for the 21272 core logic chipset for details on the PCI space mapping.

5.3.2 TIGbus Address Mapping

Table 5-2 provide the address map for the TIGbus. Refer to Table A-5 in section A.3 on page -8 for a complete list of the pinouts of the configuration jumpers which provide inputs to the TIGbus and Gpen registers.

Table 5-2 TIGbus Address Mapping

Capbus [23:21]	Physical Address 1	Access	Function	Comment
000	**800 00xx xxx0**	**RW**	**Flash ROM address space**	
001	800 08xx xxx0	RO	Gpen_0 Array0_PD[7:0]	Reserved
010	**800 10xx xxx0**	**RO**	**Gpen_1 Array1_PD[7:0]**	**Reserved**
011	800 18xx xxx0	RO	Gpen_2 Array2_PD[7:0]	Reserved
100	**800 20xx xxx0**	**RO**	**Gpen_3 Array3_PD[7:0]**	**Reserved**
101	800 28xx xxx0	RO	Gpen_4 Con_bit[7:0]	General configuration register. See Figure 5-2.
110	**800 30xx x000**	**RO**	**Gpen_5 CPU0_config[7:0]**	**CPU0 configuration register. See Figure 5-2.**
	800 30xx x040	RW	Flash write enable[0]	Writing a 1 to this location enables flash writes
	800 30xx xA00	**RW**		**Reserved**
	800 30xx xA40	RW		Reserved
	800 30xx x3C0	**RW**	**CPU[1:0] HaltA**	**Writing a 1 to either bit will halt the specified CPU.**
	800 30xx x5C0	RW	CPU[1:0] HaltB	Writing a 1 to either bit halts the specified CPU.

Table 5-2 TIGbus Address Mapping (Continued)

Capbus [23:21]	Physical Address 1	Access	Function	Comment
	800 38xx x000	**RO**	**Gpen_6 CPU1_config[7:0]**	**CPU1 configuration register. See Figure 5-2.**
	800 38xx x040	RAZ	PCI_0_ok[0]	Reserved
	800 38xx x080	**WO**	**PCI_1_ok[0]**	**PCI0 self-test register**
	800 38xx x0C0	WO		PCI1 self-test register
111	**800 38xx x100**	**RW**	**Soft_reset[0]**	**To set a hardware reset for a short period of time, first write a 0, then write a 1 to this location.**
	800 38xx x140	RO	Tig_rev[7:0]	Bits [7:5] specify the major revision (corresponding to the board revision), [4:0] specify the minor revision.
	800 38xx x180	**RO**	**Arbiter_rev[7:0]**	**Bits [7:5] specify the major**
	800 38xx x1C0	RW	Feature_mask[7:0]	Reserved

The Gpen4 register, shown in Figure 5-2, reflects the settings of the UP2000 Motherboard's switchpack 2.

7	6	5	4	3	2	1	0
Reserved	21272 speed			Mini-Debugger	CACHE_OFF_B	CACHE_OFF_A	FSB

Figure 5-2 Gpen4 Register

The Gpen5 register, shown in Figure 5-3, reflects the settings of switchpack 1 on the UP2000 Motherboard containing CPU0.

7	6	5	4	3	2	1	0
CPU0_Present_L	BC0_Config[3:0]				CPU0_Speed[2:0]		

Figure 5-3 Gpen5 Register

The Gpen6 register, shown in Figure 5-4, reflects the settings of switchpack 1 on the UP2000 Motherboard containing CPU1.

7	6	5	4	3	2	1	0
CPU1_Present_L	BC1_Config[3:0]				CPU1_Speed[2:0]		

Figure 5-4 Gpen6 Register

Appendix A

Connectors

and Pinouts

This appendix describes the connectors and pinouts used on the UP2000 Motherboard. Refer to Figure 2-1 in Chapter 2 for connector locations.

A.1 Alpha Slot B Connector Pinouts

Table A-1 describes the pinouts of the Alpha Slot B Connectors, which are standard Molex 74191-0002 parts.

Table A-1 Alpha Slot B Connector Pinouts (J22, J23)

Pin	Signal (5V, Secondary)	Signal (12V, Primary)	Signal (5V, Secondary)	Signal (12V, Primary)	Pin
A1	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B1**
A2	CONNECT	CONNECT	RESET_L	RESET_L	B2
A3	**GND**	**GND**	**GND**	**GND**	**B3**
A4	SysDataInClk_L_0	SysDataInClk_L_0	SysDataOutClk_L_0	SysDataOutClk_L_0	B4
A5	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B5**
A6	SysData_L_0	SysData_L_0	SysCheck_L_0	SysCheck_L_0	B6
A7	**GND**	**GND**	**GND**	**GND**	**B7**
A8	SysData_L_2	SysData_L_2	SysData_L_1	SysData_L_1	B8
A9	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B9**
A10	SysData_L_4	SysData_L_4	SysData_L_3	SysData_L_3	B10
A11	**GND**	**GND**	**GND**	**GND**	**B11**
A12	SysData_L_6	SysData_L_6	SysData_L_5	SysData_L_5	B12
A13	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B13**
A14	SysCheck_L_1	SysCheck_L_1	SysData_L_7	SysData_L_7	B14
A15	**GND**	**GND**	**GND**	**GND**	**B15**
A16	SysDataInClk_L_1	SysDataInClk_L_1	SysDataOutClk_L_1	SysDataOutClk_L_1	B16
A17	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B17**
A18	SysData_L_9	SysData_L_9	SysData_L_8	SysData_L_8	B18
A19	**GND**	**GND**	**GND**	**GND**	**B19**
A20	SysData_L_11	SysData_L_11	SysData_L_10	SysData_L_10	B20
A21	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B21**
A22	SysData_L_13	SysData_L_13	SysData_L_12	SysData_L_12	B22
A23	**GND**	**GND**	**GND**	**GND**	**B23**
A24	SysData_L_15	SysData_L_15	SysData_L_14	SysData_L_14	B24
A25	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B25**

Table A-1 Alpha Slot B Connector Pinouts (J22, J23) (Continued)

Pin	Signal (5V, Secondary)	Signal (12V, Primary)	Signal (5V, Secondary)	Signal (12V, Primary)	Pin
A26	SysDataInClk_L_2	SysDataInClk_L_2	SysDataOutClk_L_2	SysDataOutClk_L_2	B26
A27	**GND**	**GND**	**GND**	**GND**	**B27**
A28	SysData_L_16	SysData_L_16	SysCheck_L_2	SysCheck_L_2	B28
A29	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B29**
A30	SysData_L_18	SysData_L_18	SysData_L_17	SysData_L_17	B30
A31	**GND**	**GND**	**GND**	**GND**	**B31**
A32	SysData_L_20	SysData_L_20	SysData_L_19	SysData_L_19	B32
A33	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B33**
A34	SysData_L_22	SysData_L_22	SysData_L_21	SysData_L_21	B34
A35	**GND**	**GND**	**GND**	**GND**	**B35**
A36	SysCheck_L_3	SysCheck_L_3	SysData_L_23	SysData_L_23	B36
A37	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B37**
A38	SysDataInClk_L_3	SysDataInClk_L_3	SysDataOutClk_L_3	SysDataOutClk_L_3	B38
A39	**GND**	**GND**	**GND**	**GND**	**B39**
A40	SysData_L_25	SysData_L_25	SysData_L_24	SysData_L_24	B40
A41	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B41**
A42	SysData_L_27	SysData_L_27	SysData_L_26	SysData_L_26	B42
A43	**GND**	**GND**	**GND**	**GND**	**B43**
A44	SysData_L_29	SysData_L_29	SysData_L_28	SysData_L_28	B44
A45	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B45**
A46	SysData_L_31	SysData_L_31	SysData_L_30	SysData_L_30	B46
A47	**GND**	**GND**	**GND**	**GND**	**B47**
A48	ClkIn_H	ClkIn_H	ClkIn_L	ClkIn_L	B48
A49	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B49**
A50	FrameClk_H	FrameClk_H	FrameClk_L	FrameClk_L	B50
A51	**GND**	**GND**	**GND**	**GND**	**B51**
A52	SysDataInValid_L	SysDataInValid_L	SysDataOutValid_L	SysDataOutValid_L	B52
A53	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B53**
A54	SysFillValid_L	SysFillValid_L	ClkFwdRst_H	ClkFwdRst_H	B54
A55	**GND**	**GND**	**GND**	**GND**	**B55**
A56	PWROK	PWROK	PROCRDY_Srom_OE_L	PROCRDY/Srom_OE_L	B56
A57	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B57**
A58	SysAddIn_L_14	SysAddIn_L_14	SysAddIn_L_13	SysAddIn_L_13	B58

Table A-1 Alpha Slot B Connector Pinouts (J22, J23) (Continued)

Pin	Signal (5V, Secondary)	Signal (12V, Primary)	Signal (5V, Secondary)	Signal (12V, Primary)	Pin
A59	**GND**	**GND**	**GND**	**GND**	**B59**
A60	SysAddIn_L_12	SysAddIn_L_12	SysAddIn_L_11	SysAddIn_L_11	B60
A61	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B61**
A62	SysAddIn_L_10	SysAddIn_L_10	SysAddIn_L_9	SysAddIn_L_9	B62
A63	**GND**	**GND**	**GND**	**GND**	**B63**
A64	SysAddIn_L_8	SysAddIn_L_8	SysAddIn_L_7	SysAddIn_L_7	B64
A65	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B65**
A66	SysAddInClk_L	SysAddInClk_L	SysAddIn_L_6	SysAddIn_L_6	B66
A67	**GND**	**GND**	**GND**	**GND**	**B67**
A68	SysAddIn_L_5	SysAddIn_L_5	SysAddIn_L_4	SysAddIn_L_4	B68
A69	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B69**
A70	SysAddIn_L_3	SysAddIn_L_3	SysAddIn_L_2	SysAddIn_L_2	B70
A71	**GND**	**GND**	**GND**	**GND**	**B71**
A72	SysAddIn_L_1	SysAddIn_L_1	SysAddIn_L_0	SysAddIn_L_0	B72
A73	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B73**
A74	SysAddOut_L_14	SysAddOut_L_14	SysAddOut_L_13	SysAddOut_L_13	B74
A75	**GND**	**GND**	**GND**	**GND**	**B75**
A76	SysAddOut_L_12	SysAddOut_L_12	SysAddOut_L_11	SysAddOut_L_11	B76
A77	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B77**
A78	SysAddOut_L_10	SysAddOut_L_10	SysAddOut_L_9	SysAddOut_L_9	B78
A79	**GND**	**GND**	**GND**	**GND**	**B79**
A80	SysAddOut_L_8	SysAddOut_L_8	SysAddOut_L_7	SysAddOut_L_7	B80
A81	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B81**
A82	SysAddOutClk_L	SysAddOutClk_L	SysAddOut_L_6	SysAddOut_L_6	B82
A83	**GND**	**GND**	**GND**	**GND**	**B83**
A84	SysAddOut_L_5	SysAddOut_L_5	SysAddOut_L_4	SysAddOut_L_4	B84
A85	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B85**
A86	SysAddOut_L_3	SysAddOut_L_3	SysAddOut_L_2	SysAddOut_L_2	B86
A87	**GND**	**GND**	**GND**	**GND**	**B87**
A88	SysAddOut_L_1	SysAddOut_L_1	SysAddOut_L_0	SysAddOut_L_0	B88
A89	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B89**
A90	SysData_L_63	SysData_L_63	SysData_L_62	SysData_L_62	B90
A91	**GND**	**GND**	**GND**	**GND**	**B91**

Table A-1 Alpha Slot B Connector Pinouts (J22, J23) (Continued)

Pin	Signal (5V, Secondary)	Signal (12V, Primary)	Signal (5V, Secondary)	Signal (12V, Primary)	Pin
A92	SysData_L_61	SysData_L_61	SysData_L_60	SysData_L_60	B92
A93	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B93**
A94	SysData_L_59	SysData_L_59	SysData_L_58	SysData_L_58	B94
A95	**GND**	**GND**	**GND**	**GND**	**B95**
A96	SysData_L_57	SysData_L_57	SysData_L_56	SysData_L_56	B96
A97	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B97**
A98	SysDataInClk_L_7	SysDataInClk_L_7	SysDataOutClk_L_7	SysDataOutClk_L_7	B98
A99	**GND**	**GND**	**GND**	**GND**	**B99**
A100	SysCheck_L_7	SysCheck_L_7	SysData_L_55	SysData_L_55	B100
A101	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B101**
A102	SysData_L_54	SysData_L_54	SysData_L_53	SysData_L_53	B102
A103	**GND**	**GND**	**GND**	**GND**	**B103**
A104	SysData_L_52	SysData_L_52	SysData_L_51	SysData_L_51	B104
A105	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B105**
A106	SysData_L_50	SysData_L_50	SysData_L_49	SysData_L_49	B106
A107	**GND**	**GND**	**GND**	**GND**	**B107**
A108	SysData_L_48	SysData_L_48	SysCheck_L_6	SysCheck_L_6	B108
A109	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B109**
A110	SysDataInClk_L_6	SysDataInClk_L_6	SysDataOutClk_L_6	SysDataOutClk_L_6	B110
A111	**GND**	**GND**	**GND**	**GND**	**B111**
A112	SysData_L_47	SysData_L_47	SysData_L_46	SysData_L_46	B112
A113	**VTERM**	**VTERM**	**VTERM**	**VTERM**	**B113**
A114	SysData_L_45	SysData_L_45	SysData_L_44	SysData_L_44	B114
A115	**GND**	**GND**	**GND**	**GND**	**B115**
A116	SysData_L_43	SysData_L_43	SysData_L_42	SysData_L_42	B116
A117	**VCC_CORE**	**VCC_CORE**	**VCC_CORE**	**VCC_CORE**	**B117**
A118	SramPowerLevel	SramPowerLevel	Core_PowerGood	Core_PowerGood	B118
A119	**GND**	**GND**	**GND**	**GND**	**B119**
A120	SysData_L_41	SysData_L_41	SysData_L_40	SysData_L_40	B120
A121	**VCC**	**VCC**	**VCC**	**VCC**	**B121**
A122	SysDataInClk_L_5	SysDataInClk_L_5	SysDataOutClk_L_5	SysDataOutClk_L_5	B122
A123	**GND**	**GND**	**GND**	**GND**	**B123**
A124	SysCheck_L_5	SysCheck_L_5	SysData_L_39	SysData_L_39	B124

Table A-1 Alpha Slot B Connector Pinouts (J22, J23) (Continued)

Pin	Signal (5V, Secondary)	Signal (12V, Primary)	Signal (5V, Secondary)	Signal (12V, Primary)	Pin
A125	**VCC_SRAM**	**VCC_SRAM**	**VCC_SRAM**	**VCC_SRAM**	**B125**
A126	SysData_L_38	SysData_L_38	SysData_L_37	SysData_L_37	B126
A127	**GND**	**GND**	**GND**	**GND**	**B127**
A128	SysData_L_36	SysData_L_36	SysData_L_35	SysData_L_35	B128
A129	**V33**	**V33**	**V33**	**V33**	**B129**
A130	SysData_L_34	SysData_L_34	SysData_L_33	SysData_L_33	B130
A131	**GND**	**GND**	**GND**	**GND**	**B131**
A132	SysData_L_32	SysData_L_32	SysCheck_L_4	SysCheck_L_4	B132
A133	**V33**	**V33**	**V33**	**V33**	**B133**
A134	SysDataInClk_L_4	SysDataInClk_L_4	SysDataOutClk_L_4	SysDataOutClk_L_4	B134
A135	**GND**	**GND**	**GND**	**GND**	**B135**
A136	SromClk_H	SromClk_H	SromData_H	SromData_H	B136
A137	**V33**	**V33**	**V33**	**V33**	**B137**
A138	SRAM_ZZ	SRAM_ZZ	CORE_PWREN	CORE_PWREN	B138
A139	**GND**	**GND**	**GND**	**GND**	**B139**
A140	FIDSEL_L_0	FIDSEL_L_0	FIDSEL_L_1	FIDSEL_L_1	B140
A141	**V33**	**V33**	**V33**	**V33**	**B141**
A142	APIC_CLK	APIC_CLK	APIC_DATA_0	APIC_DATA_0	B142
A143	**VP12**	**VP12**	**VP12**	**VP12**	**B143**
A144	APIC_DATA_1	APIC_DATA_1	FERR	FERR	B144
A145	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B145**
A146	ALPHA_H/K7_L	ALPHA_H/K7_L	CPU_Present	CPU_Present	B146
A147	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B147**
A148	FID_0	FID_0	FID_1	FID_1	B148
A149	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B149**
A150	FID_2	FID_2	FID_3	FID_3	B150
A151	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B151**
A152	I2C_ADDR_0	I2C_ADDR_0	I2C_ADDR_1	I2C_ADDR_1	B152
A153	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B153**
A154	I2C_ADDR_2	I2C_ADDR_2	I2C_INTR_L	I2C_INTR_L	B154
A155	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B155**

Table A-1 Alpha Slot B Connector Pinouts (J22, J23) (Continued)

Pin	Signal (5V, Secondary)	Signal (12V, Primary)	Signal (5V, Secondary)	Signal (12V, Primary)	Pin
A156	I2C_SCLK	I2C_SCLK	I2C_SDA	I2C_SDA	B156
A157	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B157**
A158	INIT_L	INIT_L	IGNNE_L	IGNNE_L	B158
A159	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B159**
A160	IRQ_H_0/NMI	IRQ_H_0/NMI	IRQ_H_1/INTR	IRQ_H_1/INTR	B160
A161	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B161**
A162	IRQ_H_2/SMI_L	IRQ_H_2/SMI_L	IRQ_H_3/STPCLK_L	IRQ_H_3/STPCLK_L	B162
A163	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B163**
A164	IRQ_H_4/SCIINT_L	IRQ_H_4/SCIINT_L	IRQ_H_5/A20M_L	IRQ_H_5/A20M_L	B164
A165	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**VRM_SOURCE_POWER (5V)**	**VRM_SOURCE_POWER (12V)**	**B165**

A.2 Power Connector Pinouts

Pinouts for J26, the ATX power connector, are shown in Table A-2. J26 is a standard Molex 39-29-9202 connector.

Table A-2 ATX Power Connector Pinouts (J26)

Pin	Signal	Pin	Signal
1	**+3.3 VDC**	**11**	**+3.3 VDC**
2	+3.3 VDC	12	-12 VDC
3	**GND**	**13**	**GND**
4	+5 VDC	14	PS_ON
5	**GND**	**15**	**GND**
6	+5 VDC	16	GND
7	**GND**	**17**	**GND**
8	P_DCOK	18	-5 VDC
9	**5V SB**	**19**	**+5 VDC**
10	+12 VDC	20	+5 VDC

Table A-3 shows the pinouts for J28, an AUX ATX +3V power connector (PSCONN6). This part is a Molex 15-48-0412 connector.

Table A-3 AUX ATX Power Connector (PSCONN6) Pinouts (J28)

Pin	Signal	Pin	Signal
1	**GND**	**4**	**+3.3 VDC**
2	GND	5	+3.3 VDC
3	**GND**	**6**	**+5 VDC**

Pinouts for J25, the Alpha Slot B Module +12V power connector (PSCONN4), are shown in Table A-4. J25 is a Molex 15-24-4345 connector.

Table A-4 Alpha Slot B Module Power Connector (PSCONN4) Pinouts (J25)

Pin	Signal	Pin	Signal
1	**+12 VDC**	**3**	**GND**
2	GND	4	+5 VDC

A.3 Configuration Jumper Pinouts

The UP2000 Motherboard has four sets of programmable jumpers, located at J27, J29, J34, and J36 as shown in Figure 2-2 on page 2-5. Table A-5 lists the pinouts of these jumpers. J27, J29, J34 and J36 are all Molex 10-89-9167 connectors.

Table A-5Programmable Jumper Pinouts (J27, J29, J34, J36)

	Signal			
Pin	**J27**	**J29**	**J34**	**J36**
1	**Tig_Data_7**	**FSB**	**Flash_Sel2**	**BC_A_CFG0**
2	GND	GND	GND	GND
3	**Tig_Data_6**	**Cache_Off_A**	**Flash_Sel1**	**BC_A_CFG1**

Table A-5Programmable Jumper Pinouts (J27, J29, J34, J36) (Continued)

Pin	Signal			
	J27	J29	J34	J36
4	GND	GND	GND	GND
5	**Tig_Data_5**	**Cache_Off_B**	**Flash_Sel0**	**BC_A_CFG2**
6	GND	GND	GND	GND
7	**Tig_Data_4**	**Mini_Debug**	**Fl_Sel_Bypass**	**BC_A_CFG3**
8	GND	GND	GND	GND
9	**Tig_Data_3**	**Tsu_Spd0**	**CPU_SPD0**	**BC_B_CFG0**
10	GND	GND	GND	GND
11	**Tig_Data_2**	**Tsu_Spd1**	**CPU_SPD1**	**BC_B_CFG1**
12	GND	GND	GND	GND
13	**Spare**	**Tsu_Spd2**	**CPU_SPD2**	**BC_B_CFG2**
14	GND	GND	GND	GND
15	**F1_Wr_Prot_L**	**128-256**	**Spare**	**BC_B_CFG3**
16	GND	GND	GND	GND

A.4 Non-standard Connections

Some industry standard parts used in the UP2000 are connected in non-standard applications. These connections are described in the following paragraphs.

A.4.1 COM1 Connector Pinouts

Table A-6 shows the pinouts for COM1 of J5, the parallel / serial D-SUB connector. This connector is a Foxconn DM11351-Z5 part.

Table A-6 COM1 Pinout of Parallel/Serial D-SUB Connector (J5)

Pin	Name	Direction	Description
1	**CD**	←	**Carrier Detect**
2	RXD	←	Receive Data
3	**TXD**	→	**Transmit Data**
4	DTR	→	Data Terminal Ready
5	**GND**	—	**System Ground**
6	DSR	←	Data Set Ready
7	**RTS**	→	**Request to Send**
8	CTS	←	Clear to Send
9	**RST/RI**	←	**Reset/Ring Indicator**

A.4.2 Speaker Connector Pinouts

Table A-7 shows the pinouts for J41, the Speaker connector. This connector is an AMP 103239-4 part.

Table A-7 Speaker Connector Pinout (J41)

Pin	Signal	Pin	Signal
1	**Spkr_signal**	**3**	**GND**
2	+5V	4	+5V

A.4.3 Debug Port Connector Pinouts

The Alpha Slot B Module Debug Port connections are provided at J43 for the primary module, and J42 for the secondary module. Both connectors are standard AMP 103239-3 parts. Refer to Table A-8 for a complete pinout of these connectors.

Table A-8 Debug Port Connector Pinouts (J42, J43)

Pin	Signal	Pin	Signal
1	**TEST_SROM_D_L**	**3**	**SROM_CLK_L**
2	GND		

A.4.4 System Power Button Connector Pinouts

The System Power Button connector, J44, is a standard AMP 103239-2 connector. Table A-9 shows the pinouts for J44.

Table A-9 System Power Button Connector Pinout (J44)

Pin	Signal	Pin	Signal
1	**Pwr_Button**	**2**	**GND**

A.4.5 Halt Button Connector Pinouts

Table A-10 shows the pinouts for J45, the Halt Button connector. This connector is a standard AMP 103239-2 connector.

Table A-10 Halt Button Connector Pinout (J45)

Pin	Signal	Pin	Signal
1	**GND**	**2**	**Halt_Button**

A.4.6 Reset Button Connector Pinouts

The Reset Button connector, J47, is a standard AMP 103239-2 connector. Pinouts for J47 are shown in Table A-11.

Table A-11 Reset Button Connector Pinout (J47)

Pin	Signal	Pin	Signal
1	**GND**	**2**	**Reset_But_L**

A.5 Standard Connectors

Industry standard parts are used for most of the connections in the UP2000. Refer to Table A-12 for a list of the connectors used and their functions.

Table A-12 UP2000 Standard Connectors

Connector	Function	Part Number
J1, J2	**Chassis fans**	**AMP 103239-2**
J3	Keyboard and mouse	Foxconn MH11067-D2 or AMP 84405-1 or 84376-1
J4	**USB**	**AMP 787617-1**
J5	Parallel bus and COM1/COM2 serial line	Foxconn DM11351-Z5
J6	**ISA expansion bus**	**AMP 645169-3**
J7–J10	32-bit PCI bus	AMP 145154-4
J11, J12	**64-bit PCI bus**	**AMP 1-145169-2**
J13	Reset EPLD/ISP	AMP 103240-5 or Molex 10-89-9107
J14–J21	**SDRAM DIMMs**	**Berg 91159-61003**
J24	Floppy disk drive (FDD)	Molex 87256-3411 or AMP 103308-7
J30	**IDE drive bus**	**Molex 87256-4011 or AMP 103308-8**
J32	Single-ended, Ultra-wide SCSI bus	Molex 15-87-0305
J33	**LVDS/DIFF SCSI bus**	**Molex 15-87-0305**
J35, J37–J39	Alpha Slot B Module fan box power	Molex 22-23-2031
J40	**Power LED**	**AMP 103239-5**
J41	Speaker	AMP 103239-4

Table A-12 UP2000 Standard Connectors (Continued)

Connector	Function	Part Number
J42	**Primary Alpha Slot B Module SROM**	**AMP 103239-3**
J43	Secondary Alpha Slot B Module SROM	AMP 103239-3
J44	**System power button**	**AMP 103239-2**
J45	Halt button	AMP 103239-2
J46	**Ultra SCSI hard disk drive (HDD) LED**	**AMP 103239-2**
J47	Reset	AMP 103239-2

Appendix B

Support,

Products and

Documentation

B.1 Customer Support

API provides assistance for their products on their web page at www.alpha-processor.com.

Alpha Original Equipment Manufacturers (OEMs) provide the following web page resources for customer support:

URL	Description
http://www.compaq.com	**Contains links for the 21272 chipset.**
http://www.samsungsemi.com	Contains links for the 21264 CPU.

B.2 Supporting Products

API maintains a Hardware Compatibility List on their web site for components and accessories that are not included with the UP2000. Compatibility for items such as memory, power supplies, and enclosure are listed.

Point your browser to www.alpha-processor.com and check the Product Information list for Peripherals.

B.3 Alpha Products

API maintains information about other Alpha products on their web site. Point your browser to www.alpha-processor.com and check the Product Information list for Alpha products.

B.4 Documentation

B.4.1 Alpha Documentation

Title	Vendor
Alpha Architecture Reference Manual, Third Edition	**Compaq Computer Corporation, Digital Press order# EQ-W938E-DP**
Alpha Architecture Handbook, Version 4	Compaq Computer Corporation Digital Press order# EC-QD2KC-TE
AlphaPC 264DP Technical Reference Manual	**Compaq Computer Corporation, Digital Press order# EC-RBODA-TE**
UP2000 Quick Start Installation Guide (51-0030-1A)	API
***UP2000 User Guide* (51-0031-1A)**	**API**
MACASE Chassis RFI Upgrade Kit Application Note (51-0038-0A)	API

B.4.2 Third Party Documentation

You can order the following associated documentation directly from the vendor.

Title	Vendor
• ***PCI Local Bus Specification, Revision 2.1*** • ***PCI Multimedia Design Guide, Revision 1.0*** • ***PCI System Design Guide*** • ***PCI-to-PCI Bridge Architecture Specification, Revision 0*** • ***PCI BIOS Specification, Revision 2.1***	**PCI Special Interest Group** **U.S. 1-800-433-5177** **International1-503-797-4207** **FAX 1-503-234-6762**
Computer Architecture	John L. Hennessy and David A. Patterson, Morgan Kaufman Publishers, San Mateo, CA, 1990

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